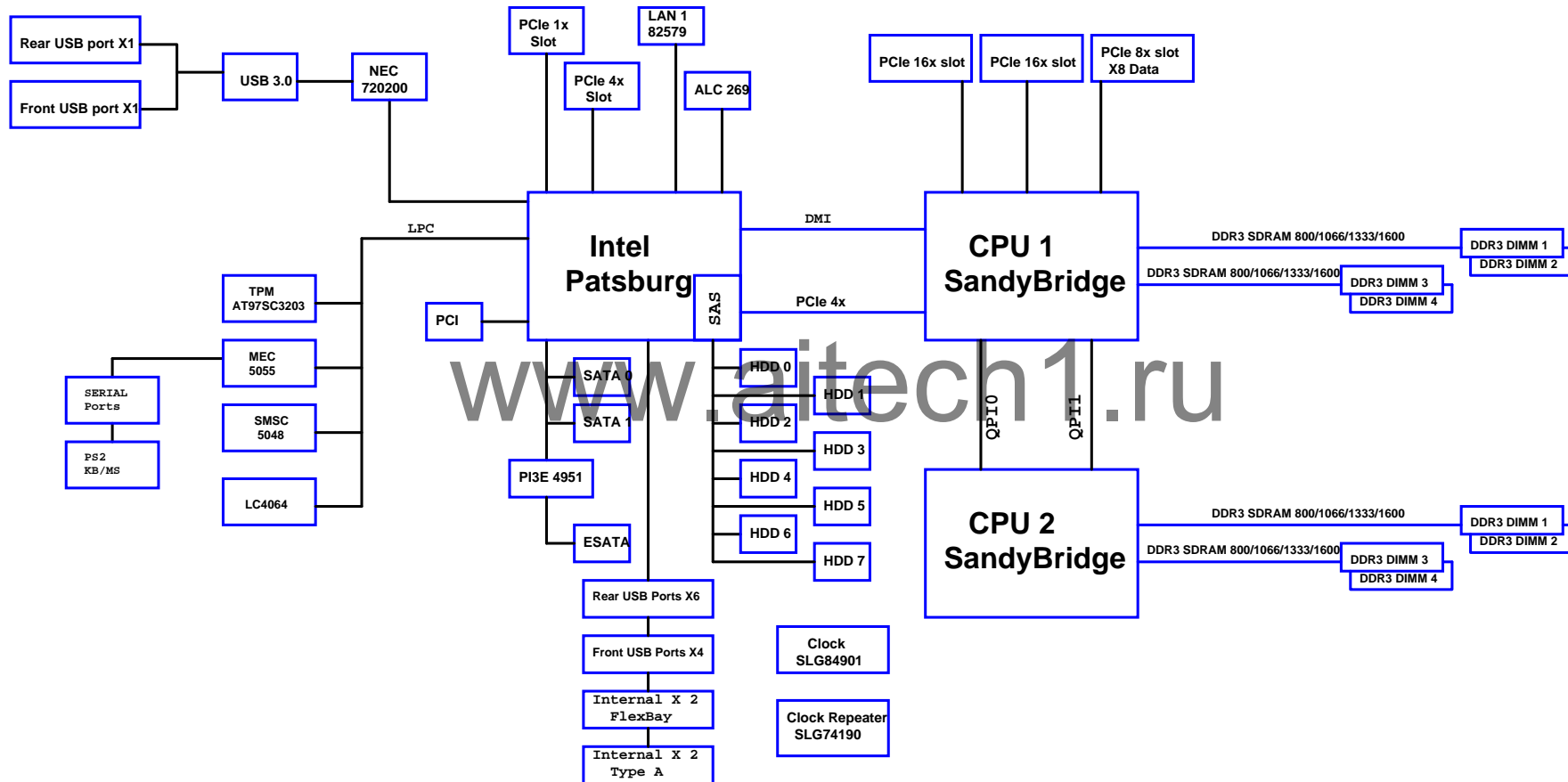
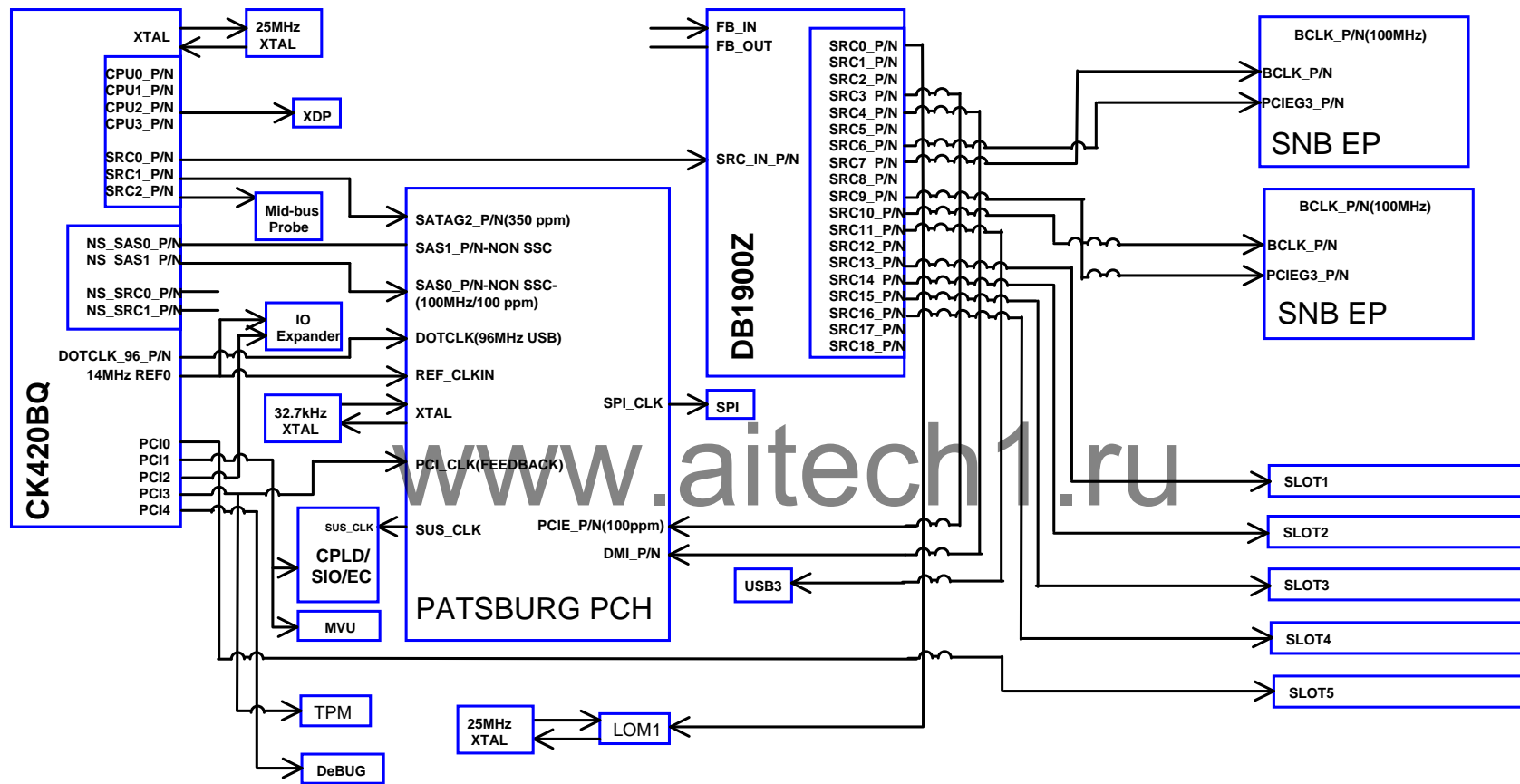
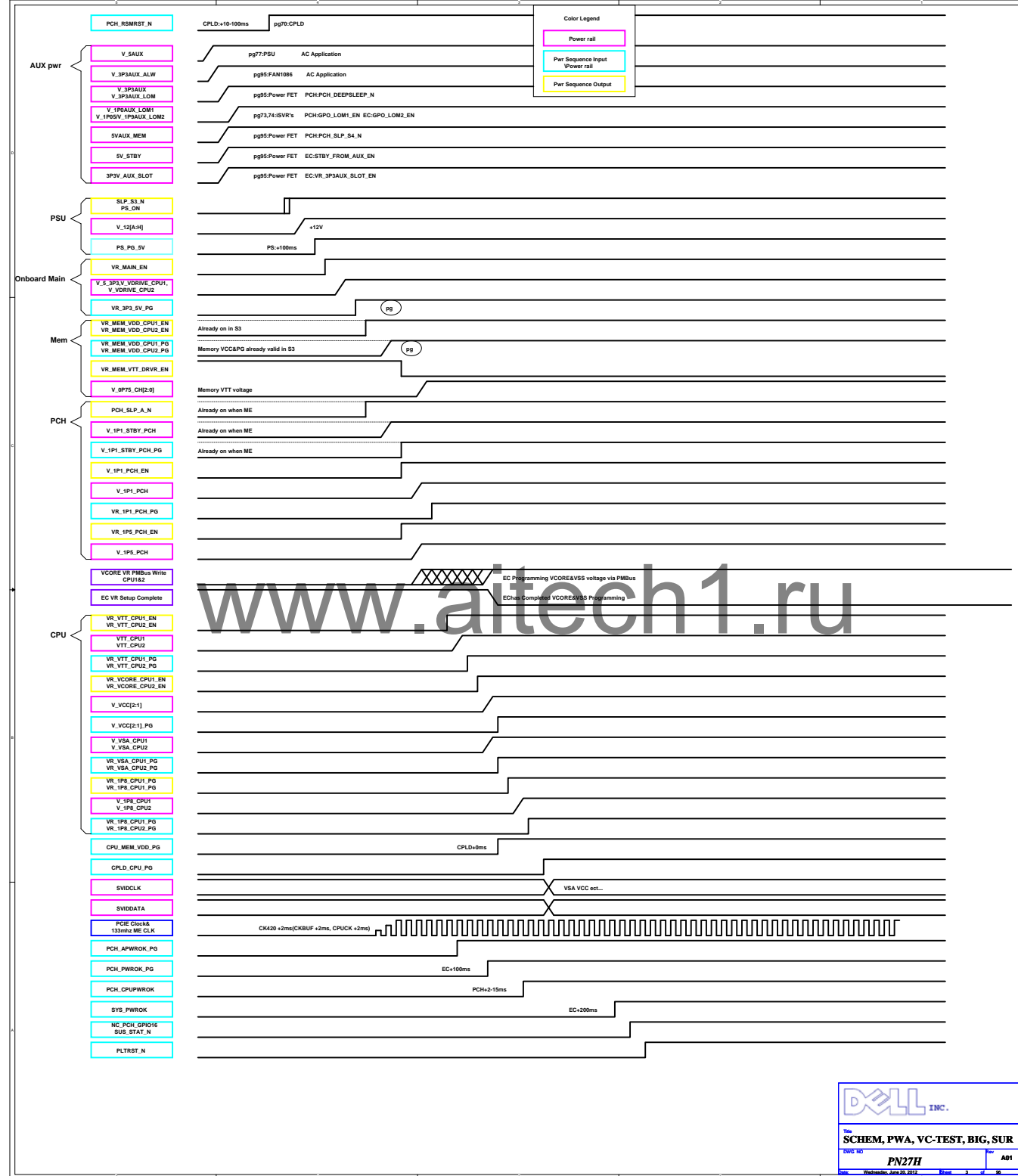


# Little Sur

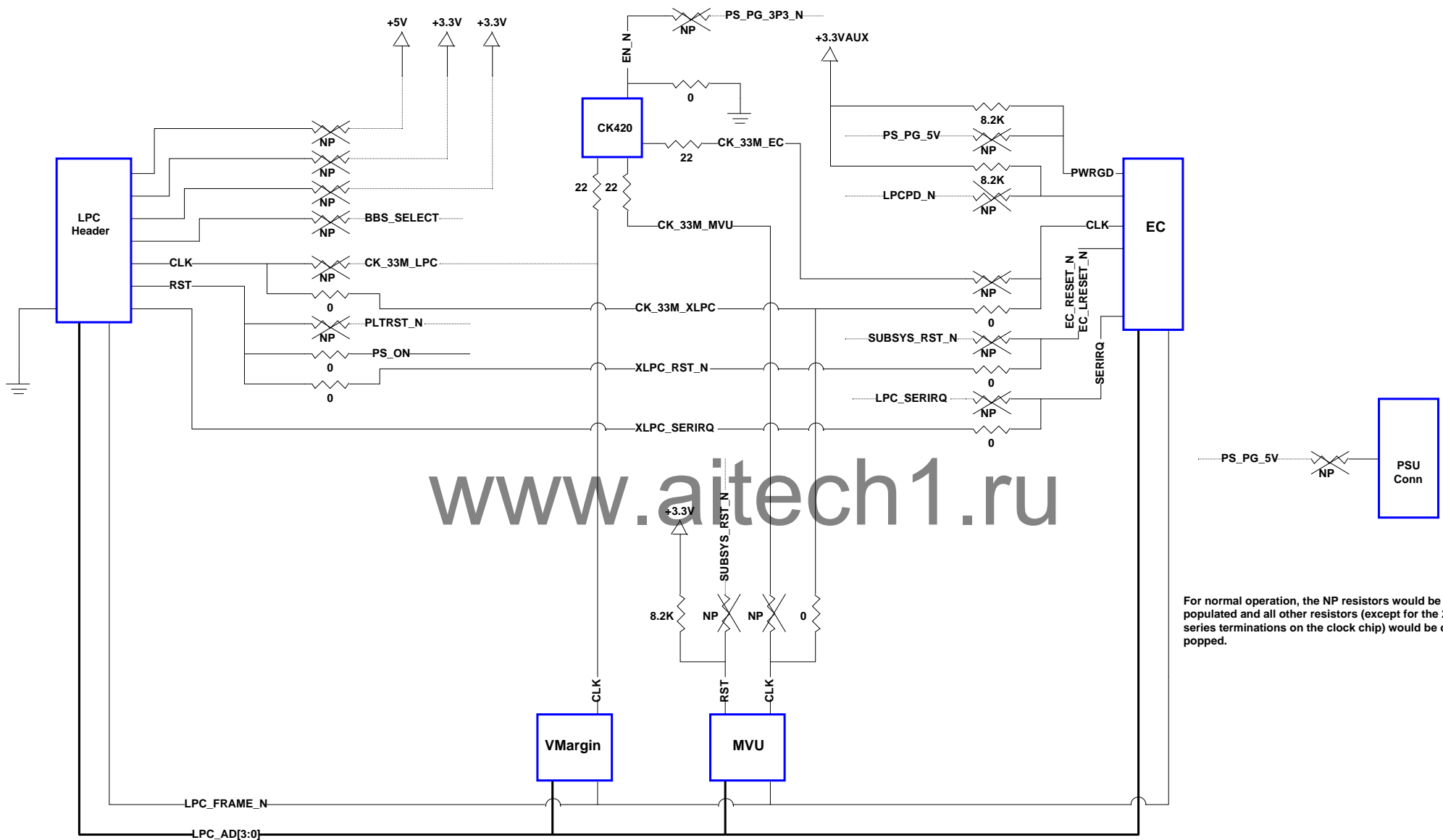









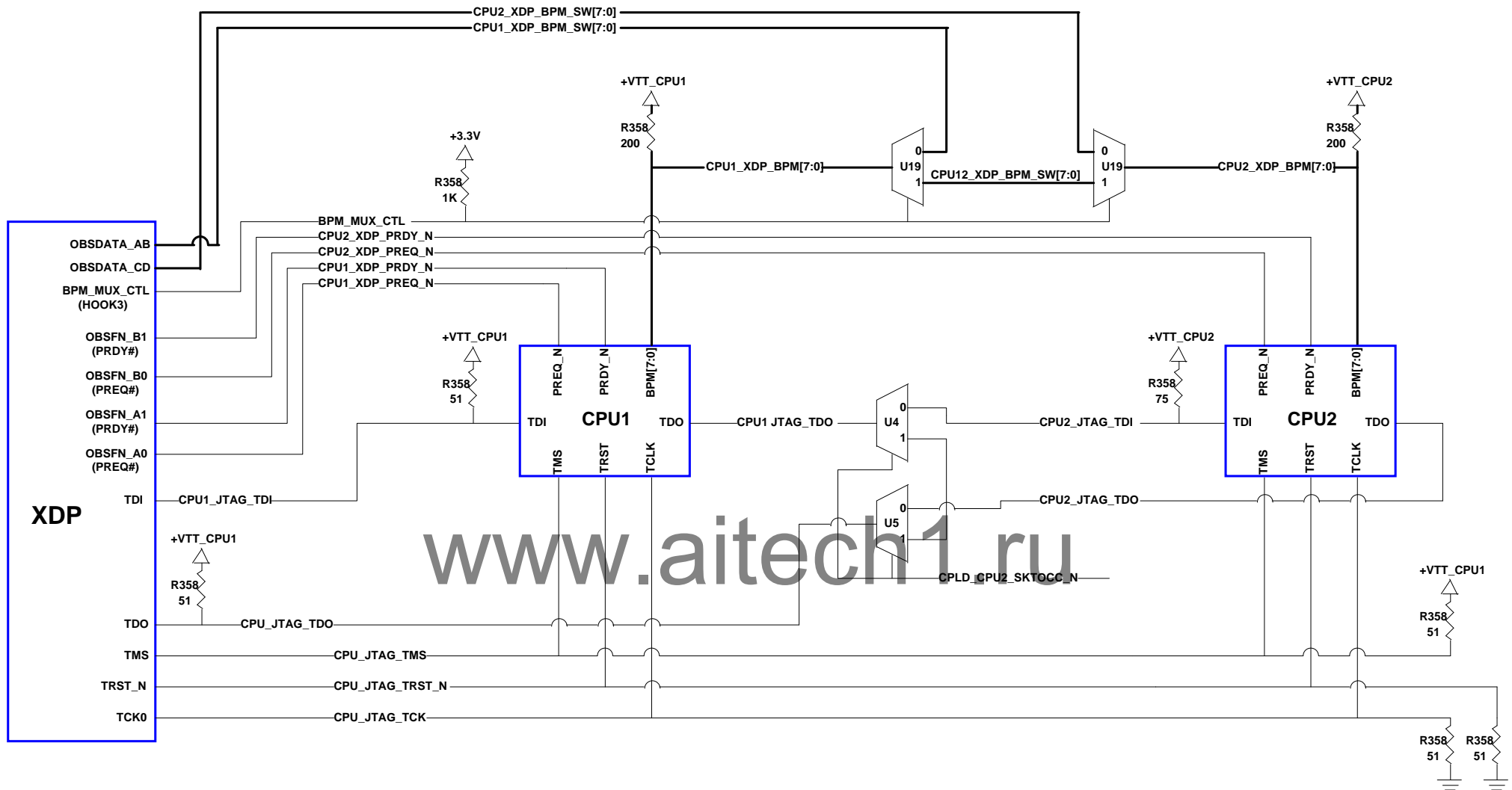




For normal operation, the NP resistors would be re-populated and all other resistors (except for the 22ohm series terminations on the clock chip) would be de-popped.

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Title <b>SCHEM, PWA, VC-TEST, BIG, SUR</b>	
DWG NO <b>PN27H</b>	Rev <b>A01</b>
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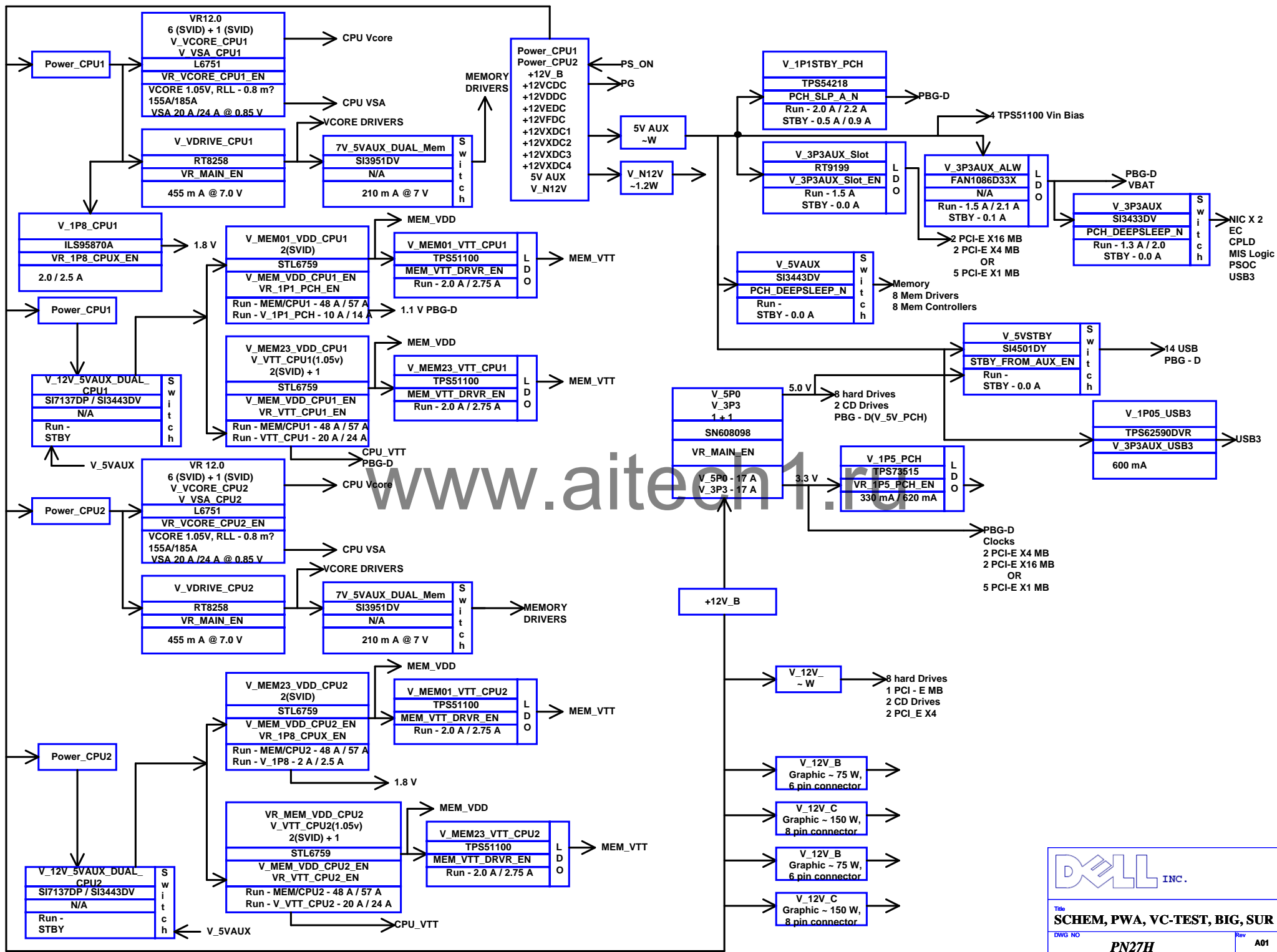


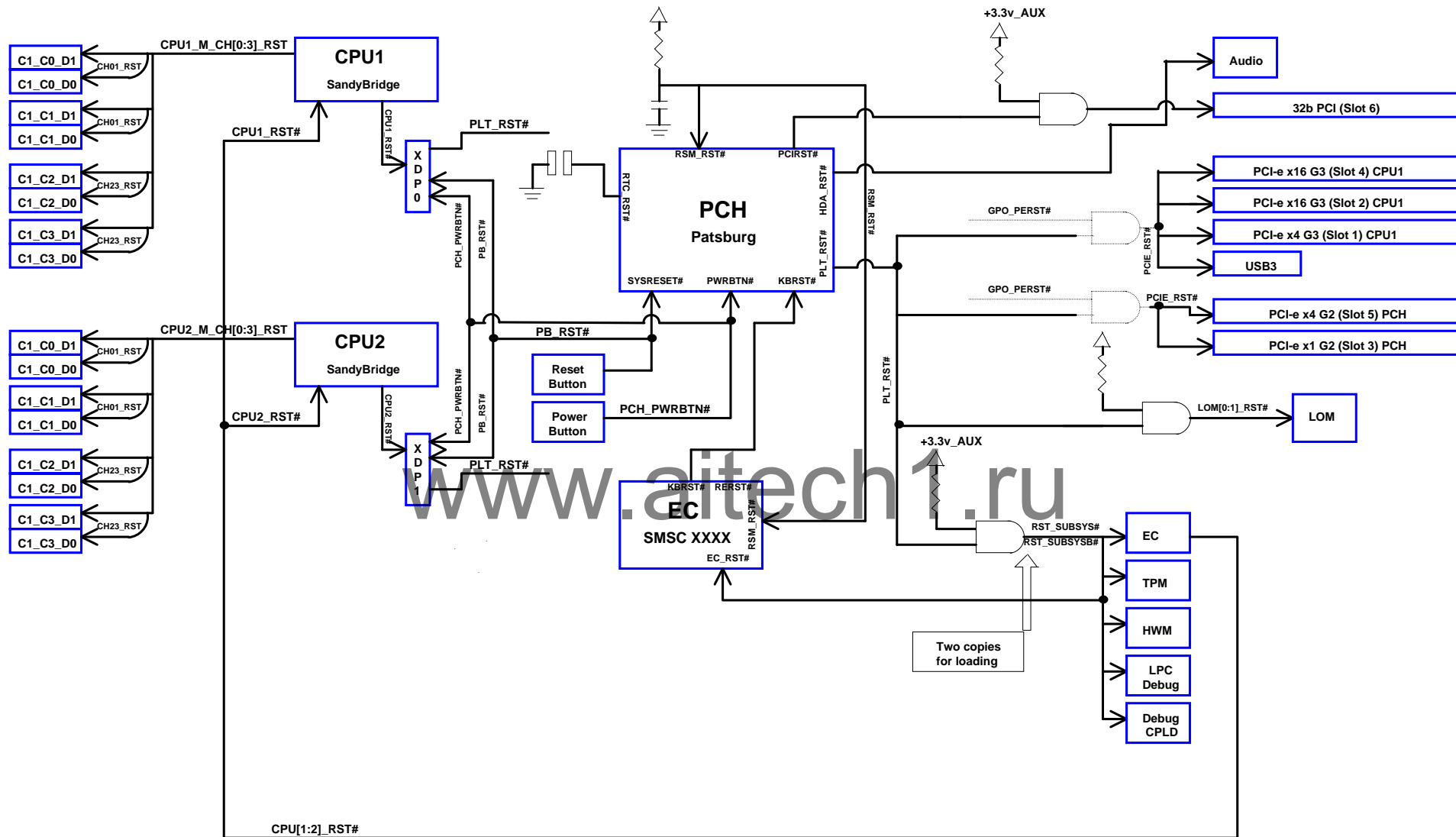
#### Debug Port Design Guide 0.95 Routing Guidelines:

- TCK/TMS max trace length = 1.5ns
- PREQ#/PRDY# max trace length = 1.5ns
- BPM max trace length between MUX and CPU = 10"
- BPM max trace length between MUXes = 8ns
- All BPM net lengths should match as a group to within +/-50ps
- All BPM nets must have 200ohm VTT terminations near CPU

#### Default settings:

- CPU1 always in scan chain
- CPU2 in scan chain if present, bypassed if not present
- PCH in separate scan chain





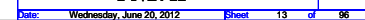








## DDR\_CH3





## QPI0 interface

CPU1I

Lane Reversed &  
DP\DN swapped  
on most lanes  
for routing

<35>	QPI CPU2, CPU1, P1P0, 00, DN	QPI CPU2, CPU1, P1P0, 00, DN	BP48	QPI0, DRX, DP, 19	QPI0, DTX, DN, 18	CE49	QPI0, CPU1, CPU2, POP1, 19, DN
<35>	QPI CPU2, CPU1, P1P0, 01, DN	QPI CPU2, CPU1, P1P0, 01, DN	B249	QPI0, DRX, DP, 18	QPI0, DTX, DN, 18	CS62	QPI0, CPU1, CPU2, POP1, 18, DN
<35>	QPI CPU2, CPU1, P1P0, 02, DN	QPI CPU2, CPU1, P1P0, 02, DN	B810	QPI0, DRX, DP, 17	QPI0, DTX, DP, 17	CS50	QPI0, CPU1, CPU2, POP1, 17, DN
<35>	QPI CPU2, CPU1, P1P0, 03, DN	QPI CPU2, CPU1, P1P0, 03, DN	B850	QPI0, DRX, DP, 16	QPI0, DTX, DP, 16	CS50	QPI0, CPU1, CPU2, POP1, 16, DN
<35>	QPI CPU2, CPU1, P1P0, 04, DN	QPI CPU2, CPU1, P1P0, 04, DN	B852	QPI0, DRX, DP, 15	QPI0, DTX, DP, 15	CE47	QPI0, CPU1, CPU2, POP1, 15, DN
<35>	QPI CPU2, CPU1, P1P0, 05, DN	QPI CPU2, CPU1, P1P0, 05, DN	B852	QPI0, DRX, DP, 14	QPI0, DTX, DP, 14	BY50	QPI0, CPU1, CPU2, POP1, 14, DN
<35>	QPI CPU2, CPU1, P1P0, 06, DN	QPI CPU2, CPU1, P1P0, 06, DN	BL53	QPI0, DRX, DP, 14	QPI0, DTX, DP, 14	BY50	QPI0, CPU1, CPU2, POP1, 13, DN
<35>	QPI CPU2, CPU1, P1P0, 07, DN	QPI CPU2, CPU1, P1P0, 07, DN	BL55	QPI0, DRX, DP, 13	QPI0, DTX, DP, 13	CA50	QPI0, CPU1, CPU2, POP1, 13, DN
<35>	QPI CPU2, CPU1, P1P0, 08, DN	QPI CPU2, CPU1, P1P0, 08, DN	BL56	QPI0, DRX, DP, 12	QPI0, DTX, DP, 12	CA50	QPI0, CPU1, CPU2, POP1, 12, DN
<35>	QPI CPU2, CPU1, P1P0, 09, DN	QPI CPU2, CPU1, P1P0, 09, DN	B656	QPI0, DRX, DP, 11	QPI0, DTX, DP, 11	CD46	QPI0, CPU1, CPU2, POP1, 10, DN
<35>	QPI CPU2, CPU1, P1P0, 10, DN	QPI CPU2, CPU1, P1P0, 10, DN	B657	QPI0, DRX, DP, 11	QPI0, DTX, DP, 11	CD46	QPI0, CPU1, CPU2, POP1, 10, DN
<35>	QPI CPU2, CPU1, P1P0, 11, DN	QPI CPU2, CPU1, P1P0, 11, DN	B657	QPI0, DRX, DP, 9	QPI0, DTX, DP, 9	BV66	QPI0, CPU1, CPU2, POP1, 09, DN
<35>	QPI CPU2, CPU1, P1P0, 12, DN	QPI CPU2, CPU1, P1P0, 12, DN	B858	QPI0, DRX, DP, 8	QPI0, DTX, DP, 8	BV66	QPI0, CPU1, CPU2, POP1, 07, DN
<35>	QPI CPU2, CPU1, P1P0, 13, DN	QPI CPU2, CPU1, P1P0, 13, DN	BF58	QPI0, DRX, DP, 7	QPI0, DTX, DP, 7	BV66	QPI0, CPU1, CPU2, POP1, 07, DN
<35>	QPI CPU2, CPU1, P1P0, 14, DN	QPI CPU2, CPU1, P1P0, 14, DN	BF58	QPI0, DRX, DP, 6	QPI0, DTX, DP, 6	BT58	QPI0, CPU1, CPU2, POP1, 06, DN
<35>	QPI CPU2, CPU1, P1P0, 15, DN	QPI CPU2, CPU1, P1P0, 15, DN	BF56	QPI0, DRX, DP, 5	QPI0, DTX, DP, 5	BU55	QPI0, CPU1, CPU2, POP1, 04, DN
<35>	QPI CPU2, CPU1, P1P0, 16, DN	QPI CPU2, CPU1, P1P0, 16, DN	BF56	QPI0, DRX, DP, 4	QPI0, DTX, DP, 4	BU55	QPI0, CPU1, CPU2, POP1, 04, DN
<35>	QPI CPU2, CPU1, P1P0, 17, DN	QPI CPU2, CPU1, P1P0, 17, DN	BF53	QPI0, DRX, DP, 3	QPI0, DTX, DP, 3	BU53	QPI0, CPU1, CPU2, POP1, 03, DN
<35>	QPI CPU2, CPU1, P1P0, 18, DN	QPI CPU2, CPU1, P1P0, 18, DN	BF51	QPI0, DRX, DP, 2	QPI0, DTX, DP, 2	BV52	QPI0, CPU1, CPU2, POP1, 01, DN
<35>	QPI CPU2, CPU1, P1P0, 19, DN	QPI CPU2, CPU1, P1P0, 19, DN	BG52	QPI0, DRX, DP, 1	QPI0, DTX, DP, 1	BV50	QPI0, CPU1, CPU2, POP1, 00, DN
<35>	QPI CPU2, CPU1, P1P0, 00, DP	QPI CPU2, CPU1, P1P0, 00, DP	BM48	QPI0, DRX, DN, 19	QPI0, DTX, DN, 19	CG49	QPI0, CPU1, CPU2, POP1, 19, DN
<35>	QPI CPU2, CPU1, P1P0, 01, DP	QPI CPU2, CPU1, P1P0, 01, DP	B249	QPI0, DRX, DN, 18	QPI0, DTX, DN, 18	CS62	QPI0, CPU1, CPU2, POP1, 18, DN
<35>	QPI CPU2, CPU1, P1P0, 02, DP	QPI CPU2, CPU1, P1P0, 02, DP	B810	QPI0, DRX, DN, 17	QPI0, DTX, DN, 17	CS50	QPI0, CPU1, CPU2, POP1, 17, DN
<35>	QPI CPU2, CPU1, P1P0, 03, DP	QPI CPU2, CPU1, P1P0, 03, DP	BP50	QPI0, DRX, DN, 15	QPI0, DTX, DN, 15	CS50	QPI0, CPU1, CPU2, POP1, 16, DN
<35>	QPI CPU2, CPU1, P1P0, 04, DN	QPI CPU2, CPU1, P1P0, 04, DN	BP52	QPI0, DRX, DN, 17	QPI0, DTX, DN, 15	CF48	QPI0, CPU1, CPU2, POP1, 16, DN
<35>	QPI CPU2, CPU1, P1P0, 05, DN	QPI CPU2, CPU1, P1P0, 05, DN	BP52	QPI0, DRX, DN, 15	QPI0, DTX, DN, 15	CE47	QPI0, CPU1, CPU2, POP1, 15, DN
<35>	QPI CPU2, CPU1, P1P0, 06, DN	QPI CPU2, CPU1, P1P0, 06, DN	BN53	QPI0, DRX, DN, 14	QPI0, DTX, DN, 14	CA49	QPI0, CPU1, CPU2, POP1, 13, DN
<35>	QPI CPU2, CPU1, P1P0, 07, DN	QPI CPU2, CPU1, P1P0, 07, DN	BP53	QPI0, DRX, DN, 14	QPI0, DTX, DN, 14	CA47	QPI0, CPU1, CPU2, POP1, 13, DN
<35>	QPI CPU2, CPU1, P1P0, 08, DN	QPI CPU2, CPU1, P1P0, 08, DN	BP56	QPI0, DRX, DN, 12	QPI0, DTX, DN, 12	BV52	QPI0, CPU1, CPU2, POP1, 13, DN
<35>	QPI CPU2, CPU1, P1P0, 09, DN	QPI CPU2, CPU1, P1P0, 09, DN	BP56	QPI0, DRX, DN, 11	QPI0, DTX, DN, 11	CF46	QPI0, CPU1, CPU2, POP1, 10, DN
<35>	QPI CPU2, CPU1, P1P0, 10, DN	QPI CPU2, CPU1, P1P0, 10, DN					

OP10\_CLKTXD, DN  
OP10\_CLKTXD, DN

CE45\_OPI\_CPU1\_CPU2\_P0P1\_CK\_DP  
CE45\_OPI\_CPU1\_CPU2\_P0P1\_CK\_DP

OPI\_CPU1\_CPU2\_P0P1\_CK\_DP  
OPI\_CPU1\_CPU2\_P0P1\_CK\_DP

<S> <S> OPI\_CPU2\_CPU1\_P0P1\_CK\_DP  
<S> <S> OPI\_CPU2\_CPU1\_P0P1\_CK\_DP

OPI\_CPU2\_CPU1\_P0P1\_CK\_DP  
OPI\_CPU2\_CPU1\_P0P1\_CK\_DP

CR55  
CR55

OP10\_CLKTXD, DN  
OP10\_CLKTXD, DN

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## QPI1 interface

CPU1J

Lane Reversed &  
DP\DN swapped  
on most lanes  
for routing

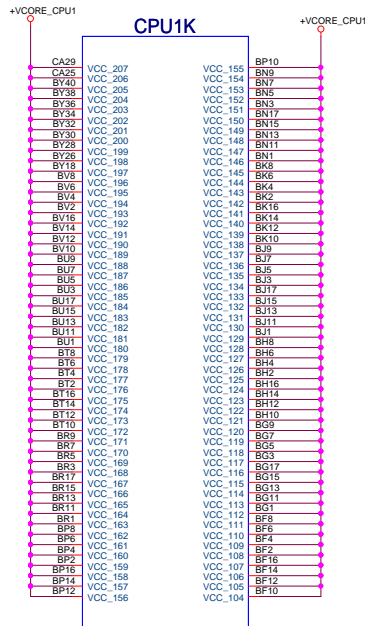
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**Title**  
**SCHEM, PWA, LITTLE, SUR**

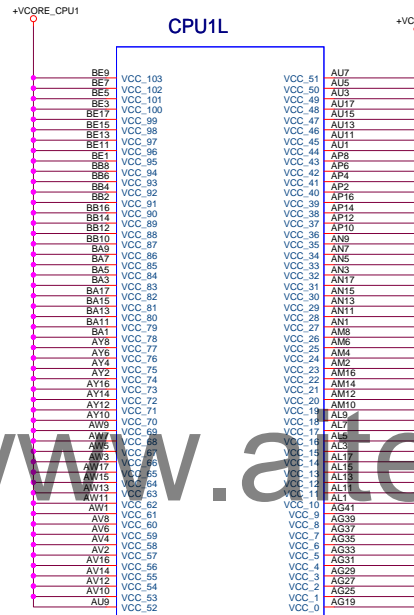
**PN27H**

A01



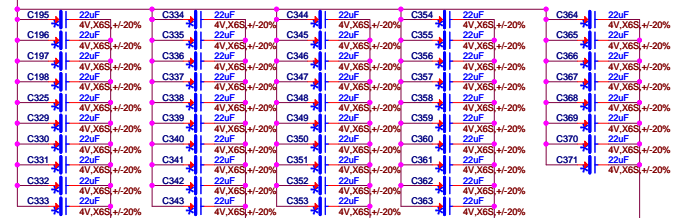


RoseCity-PG31



RoseCity-PG31

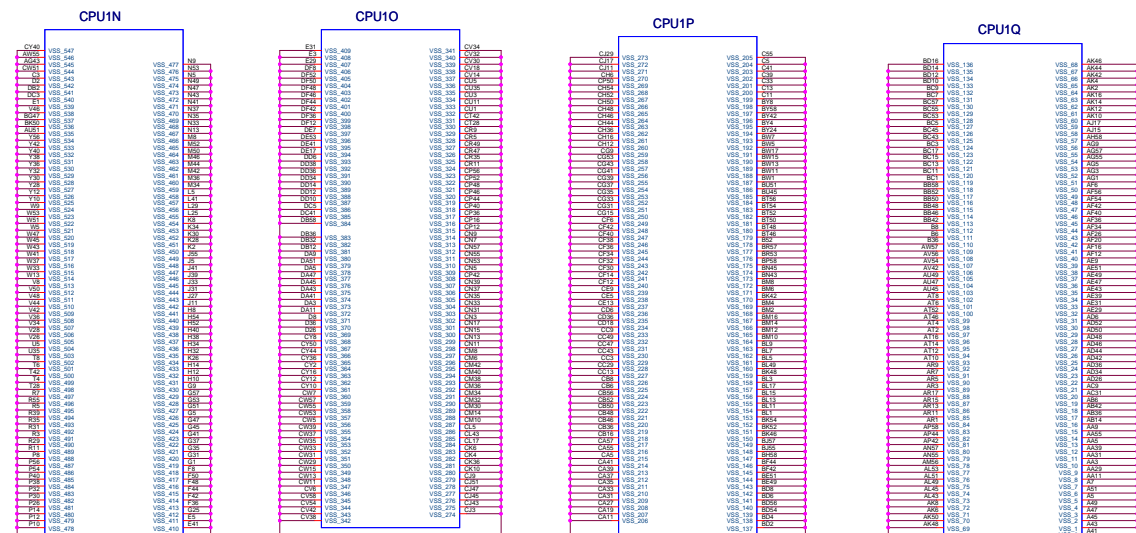
Hight Temp X6S Caps. Place in CPU cavity



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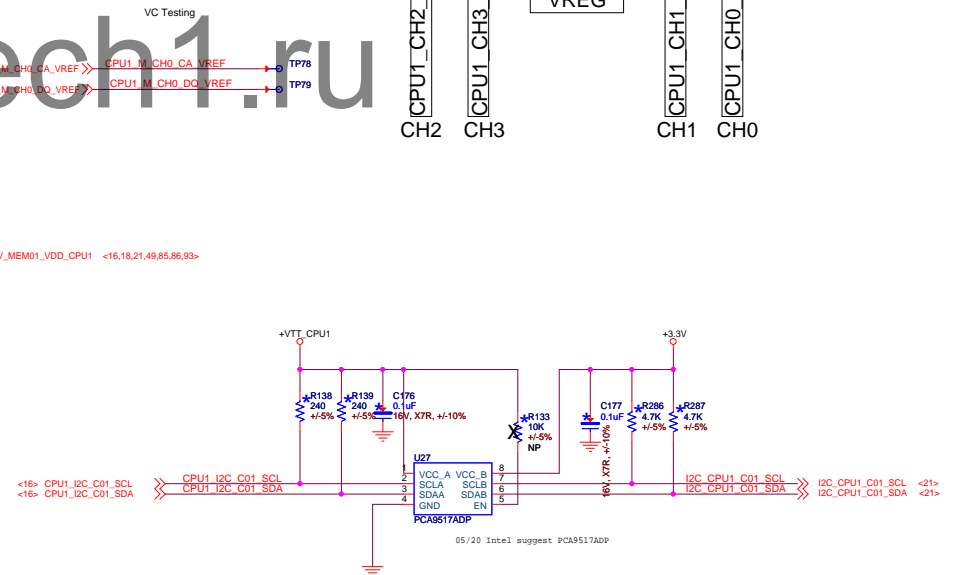
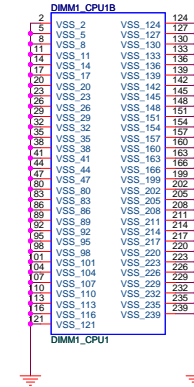
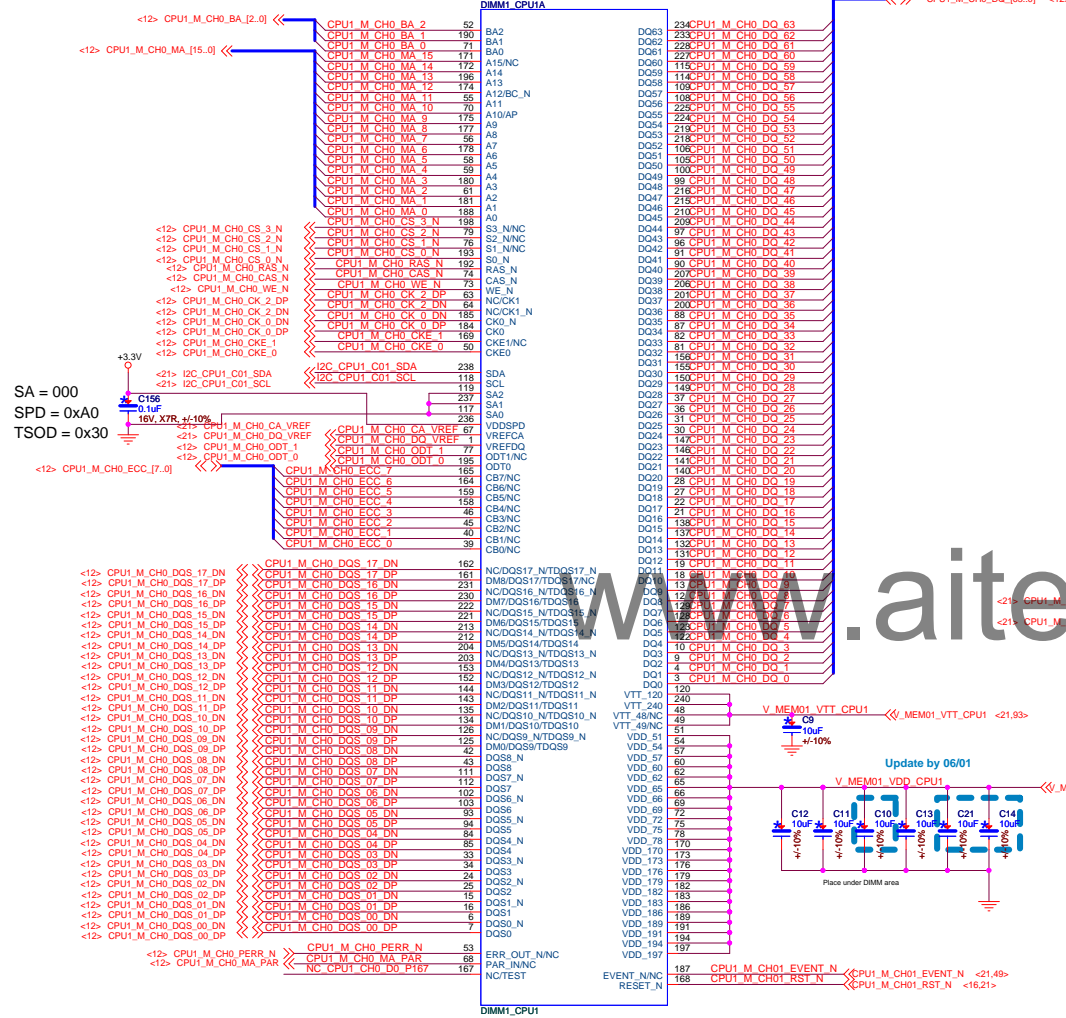






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## CPU1\_CH0\_D0



**Title**  
**SCHEM, PWA, LITTLE, SUR**

DWG NO	Rev
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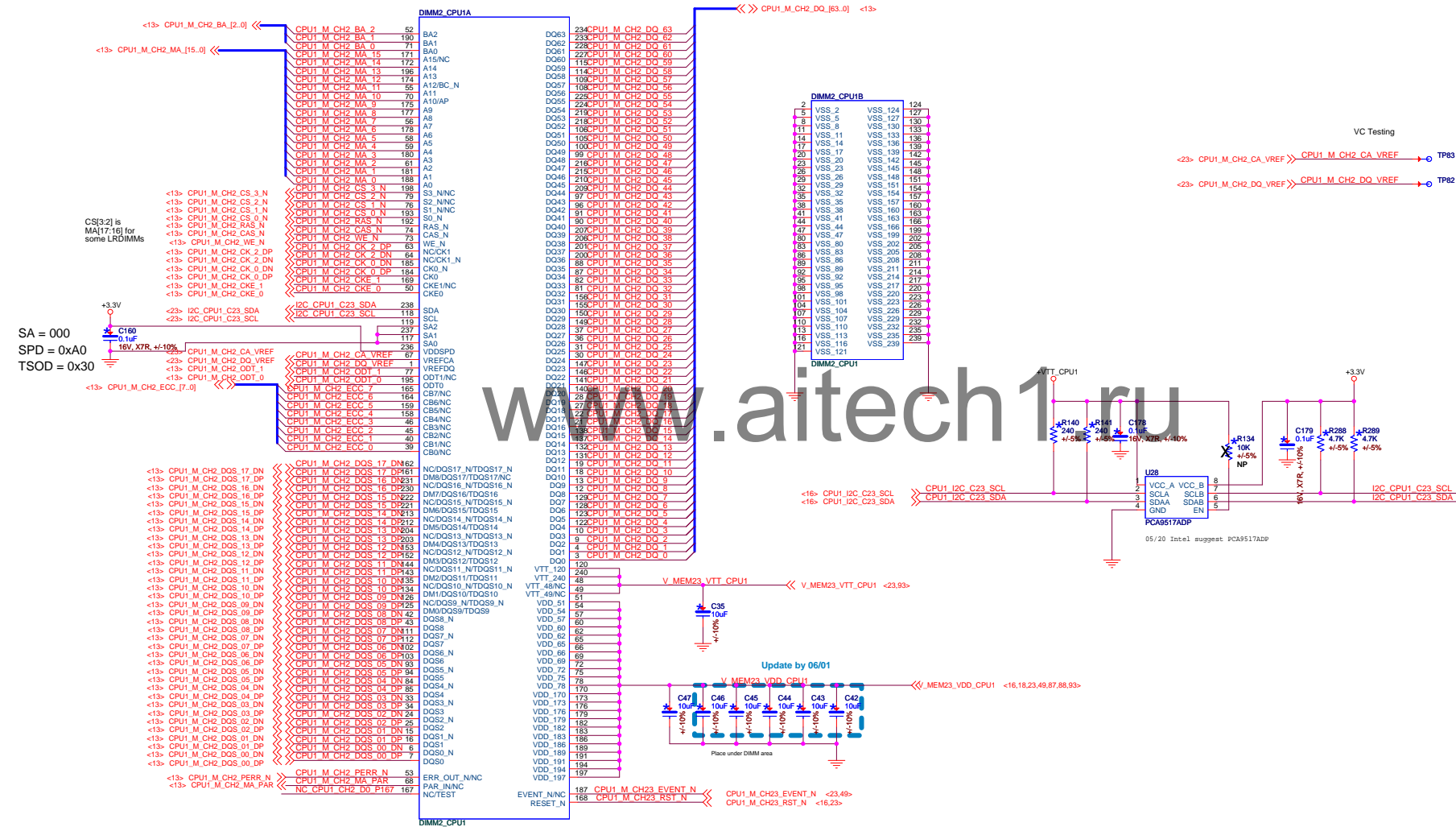
DIMM3\_CPU1A



**PN27H**

A01

## CPU1\_CH2\_D0

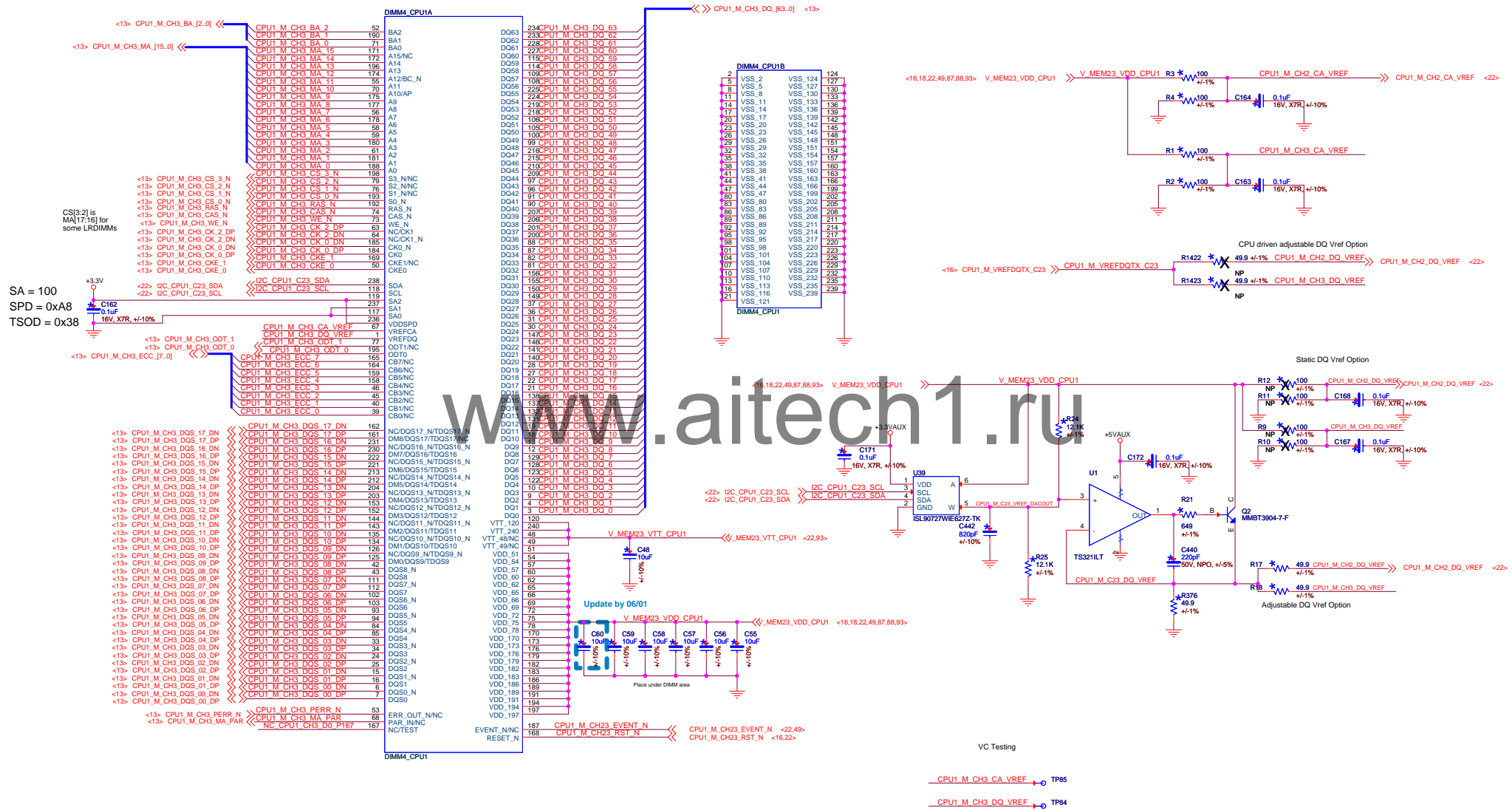


**Title**  
**SCHEM, PWA, LITTLE, SUR**

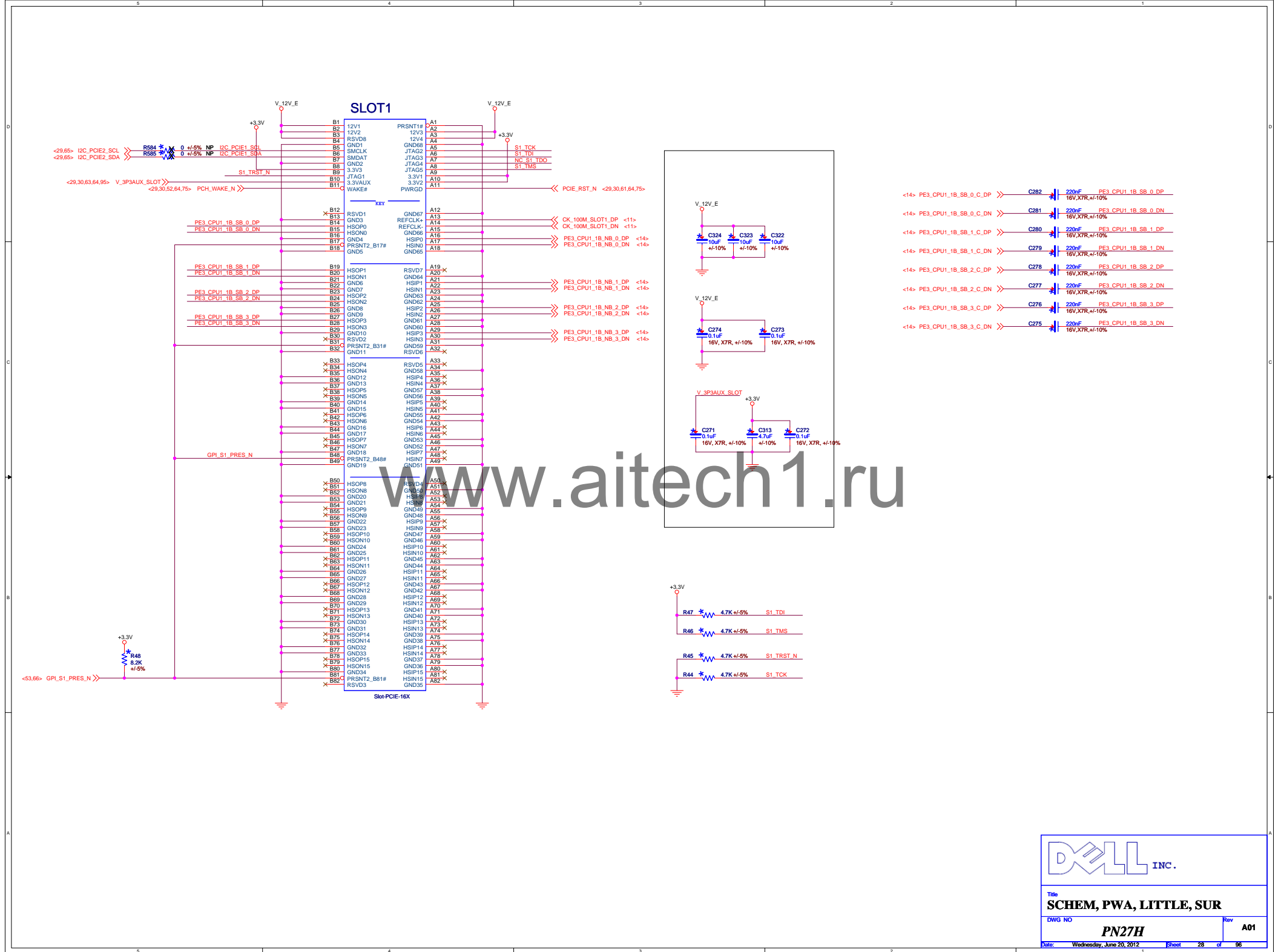
DWG NO	<b><i>PN27H</i></b>	Rev	<b>A01</b>
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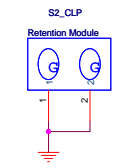
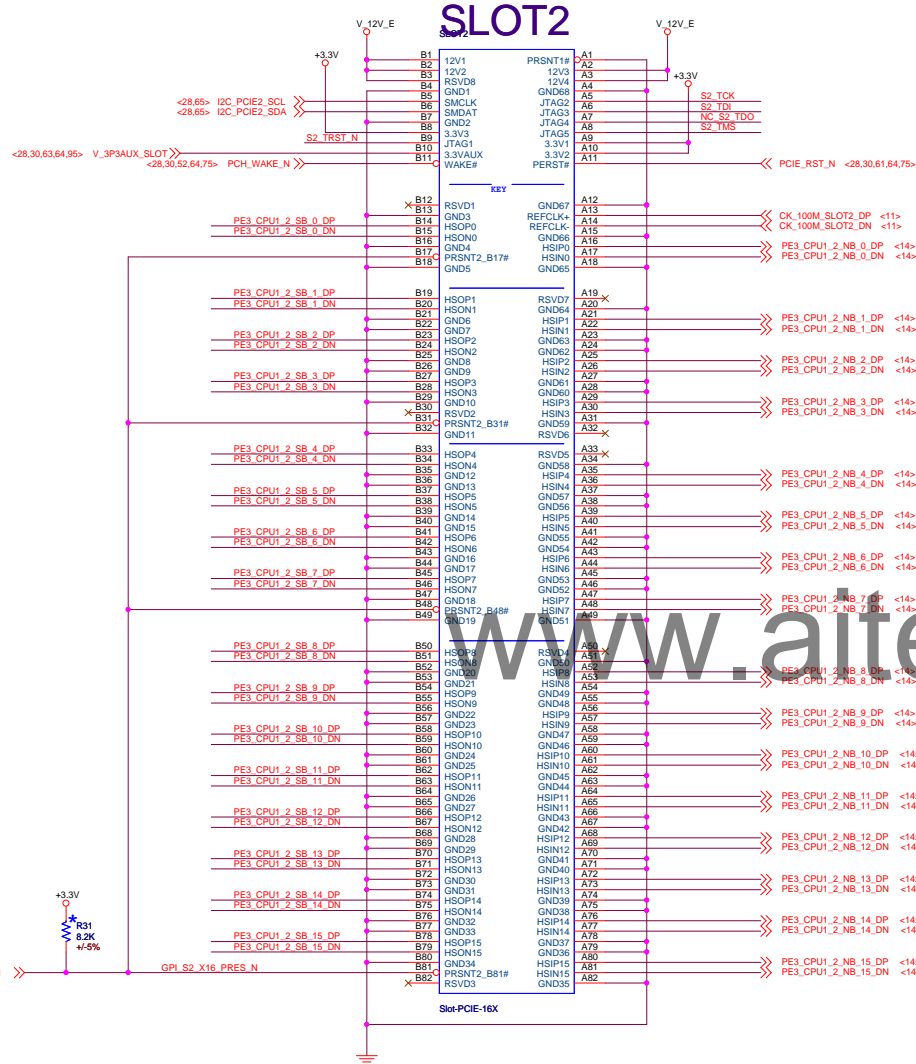
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## CPU1\_CH3\_D0

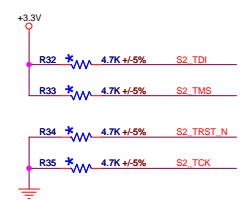
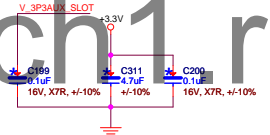
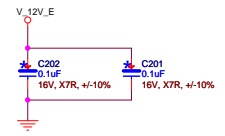
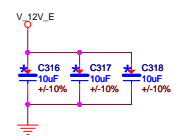


Title		SCHEM, PWA, LITTLE, SUR	
DWG NO	<b>PN27H</b>	Rev	<b>A01</b>
Date:	Wednesday June 20 2012	Sheet	23 of 96



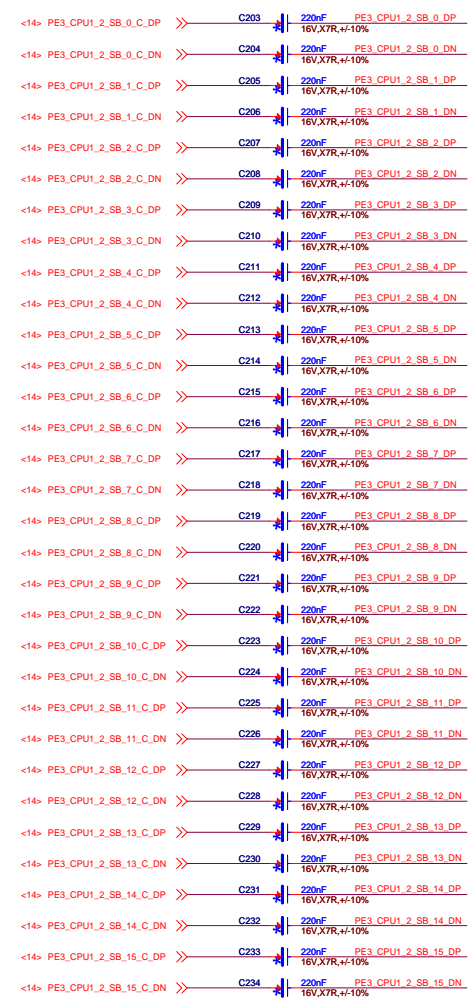


PCI-E x16 slot decoupling

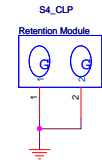
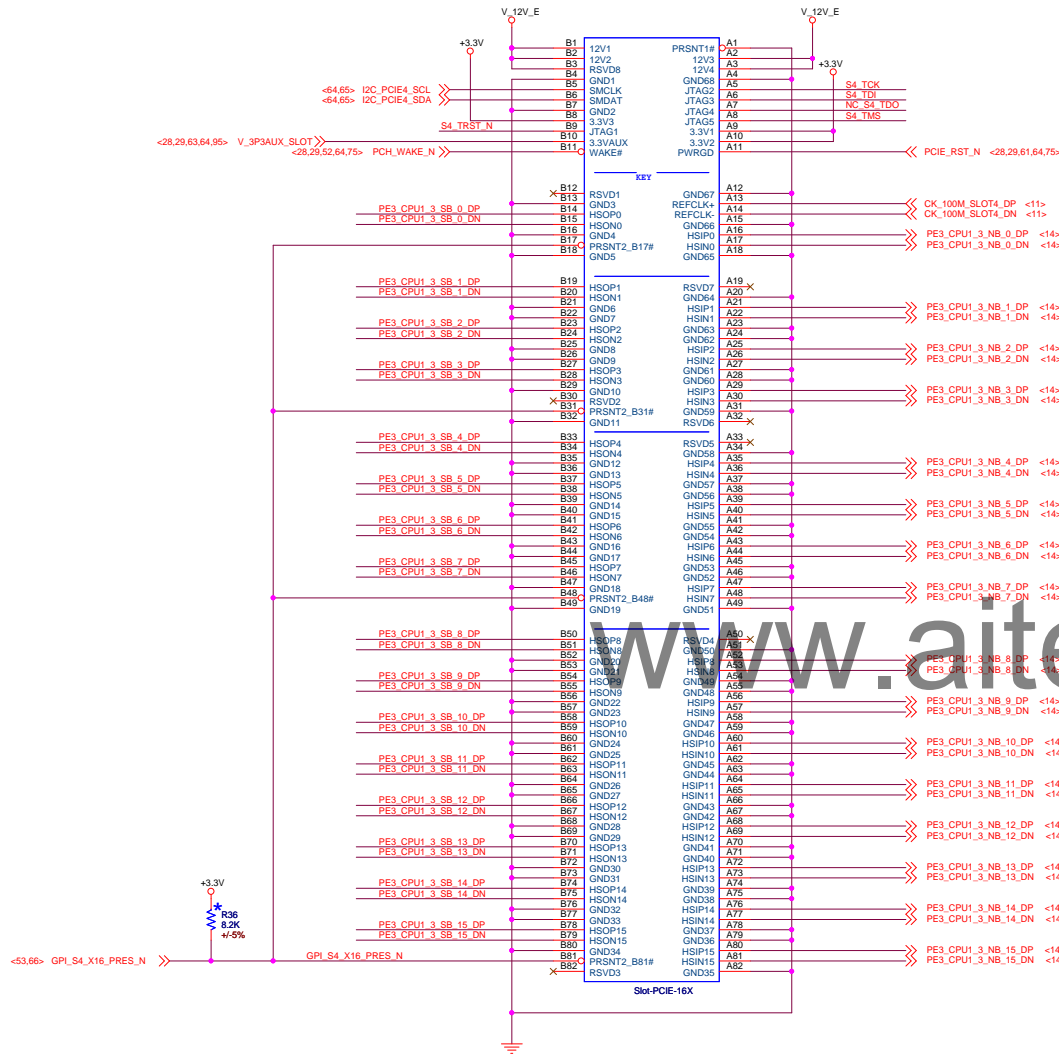


NOTE: PCIe naming convention is:  
EXP\_[UpstreamDevice]\_Port\_[NVSB]\_[LANE]\_[C]\_[DP/DN]

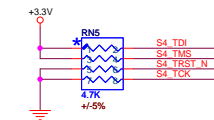
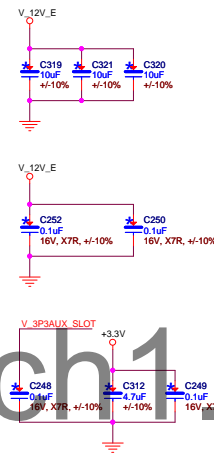
Placed by SLOT



# SLOT4

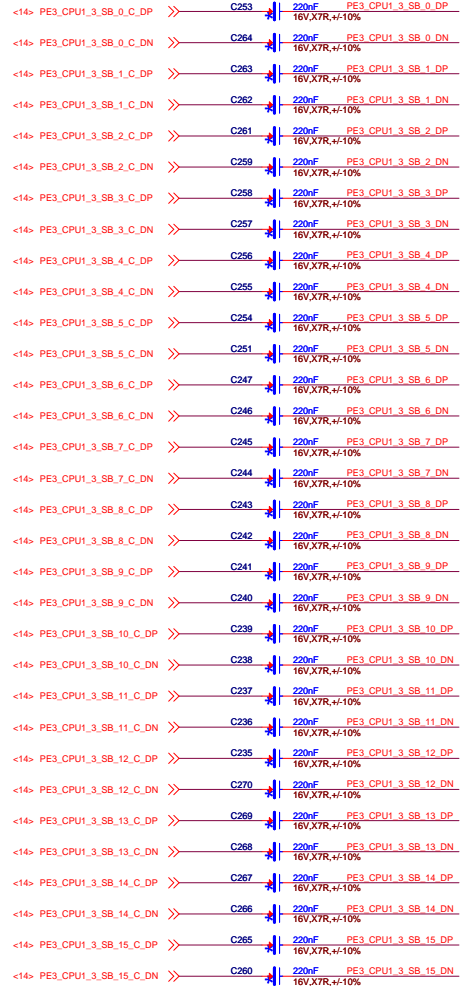


## PCI-E x16 slot decoupling



NOTE: PCIe naming convention is:  
EXP\_[UpstreamDevice]\_Port\_[NVS]B[LANE]\_[DP]DN

## Placed by SLOT







## DDR\_CH0

CPU2B

&lt;&lt;40&gt; CPU2\_M.CH0\_DQ\_[B3..0]

CPU2 M.CH0 DQ 63 CL41  
CPU2 M.CH0 DQ 62 CL37  
CPU2 M.CH0 DQ 61 CL37  
CPU2 M.CH0 DQ 60 CL37  
CPU2 M.CH0 DQ 59 CL42  
CPU2 M.CH0 DQ 58 CL42  
CPU2 M.CH0 DQ 57 CL38  
CPU2 M.CH0 DQ 56 CL38  
CPU2 M.CH0 DQ 55 CL38  
CPU2 M.CH0 DQ 54 CC41  
CPU2 M.CH0 DQ 53 CE37  
CPU2 M.CH0 DQ 52 CC42  
CPU2 M.CH0 DQ 51 CC42  
CPU2 M.CH0 DQ 50 CE41  
CPU2 M.CH0 DQ 49 CC42  
CPU2 M.CH0 DQ 48 CB38  
CPU2 M.CH0 DQ 47 CH34  
CPU2 M.CH0 DQ 46 CK34  
CPU2 M.CH0 DQ 45 CH30  
CPU2 M.CH0 DQ 44 CK30  
CPU2 M.CH0 DQ 43 CL35  
CPU2 M.CH0 DQ 42 CL35  
CPU2 M.CH0 DQ 41 CL31  
CPU2 M.CH0 DQ 40 CL31  
CPU2 M.CH0 DQ 39 CB34  
CPU2 M.CH0 DQ 38 CB34  
CPU2 M.CH0 DQ 37 CB30  
CPU2 M.CH0 DQ 36 CB30  
CPU2 M.CH0 DQ 35 CE35  
CPU2 M.CH0 DQ 34 CC31  
CPU2 M.CH0 DQ 33 CC31  
CPU2 M.CH0 DQ 32 CF10  
CPU2 M.CH0 DQ 31 CH10  
CPU2 M.CH0 DQ 30 CH10  
CPU2 M.CH0 DQ 29 CA9  
CPU2 M.CH0 DQ 28 BW9  
CPU2 M.CH0 DQ 27 CD12  
CPU2 M.CH0 DQ 26 BY12  
CPU2 M.CH0 DQ 25 BY10  
CPU2 M.CH0 DQ 24 BY10  
CPU2 M.CH0 DQ 23 CL15  
CPU2 M.CH0 DQ 22 CL15  
CPU2 M.CH0 DQ 21 CL11  
CPU2 M.CH0 DQ 20 CM16  
CPU2 M.CH0 DQ 19 CM16  
CPU2 M.CH0 DQ 18 CK16  
CPU2 M.CH0 DQ 17 CM12  
CPU2 M.CH0 DQ 16 CK12  
CPU2 M.CH0 DQ 15 CG5  
CPU2 M.CH0 DQ 14 CG5  
CPU2 M.CH0 DQ 13 CA3  
CPU2 M.CH0 DQ 12 CA1  
CPU2 M.CH0 DQ 11 C15  
CPU2 M.CH0 DQ 10 CH4  
CPU2 M.CH0 DQ 9 CB4  
CPU2 M.CH0 DQ 8 CB2  
CPU2 M.CH0 DQ 7 CL7  
CPU2 M.CH0 DQ 6 C37  
CPU2 M.CH0 DQ 5 CA7  
CPU2 M.CH0 DQ 4 BY6  
CPU2 M.CH0 DQ 3 CL9  
CPU2 M.CH0 DQ 2 CK8  
CPU2 M.CH0 DQ 1 CB8  
CPU2 M.CH0 DQ 0 CC7

CK29  
CL27  
CC26  
CB28  
CP26  
CG27  
CB28  
CC25  
CN25  
CH22  
CG24  
CG24  
CH24  
CF22  
CE24  
CE24  
CF24

DDR0\_CS\_N\_9  
DDR0\_CS\_N\_8  
DDR0\_CS\_N\_7  
DDR0\_CS\_N\_6  
DDR0\_CS\_N\_5  
DDR0\_CS\_N\_4  
DDR0\_CS\_N\_3  
DDR0\_CS\_N\_2  
DDR0\_CS\_N\_1  
DDR0\_CS\_N\_0  
DDR0\_CLK\_DP\_3  
DDR0\_CLK\_DP\_2  
DDR0\_CLK\_DP\_1  
DDR0\_CLK\_DP\_0  
DDR0\_CLK\_DN\_3  
DDR0\_CLK\_DN\_2  
DDR0\_CLK\_DN\_1  
DDR0\_CLK\_DN\_0

DDR0\_DQS\_DP\_17  
DDR0\_DQS\_DP\_16  
DDR0\_DQS\_DP\_15  
DDR0\_DQS\_DP\_14  
DDR0\_DQS\_DP\_13  
DDR0\_DQS\_DP\_12  
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DDR0\_DQS\_DP\_3  
DDR0\_DQS\_DP\_2  
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DDR0\_DQS\_DN\_17  
DDR0\_DQS\_DN\_16  
DDR0\_DQS\_DN\_15  
DDR0\_DQS\_DN\_14  
DDR0\_DQS\_DN\_13  
DDR0\_DQS\_DN\_12  
DDR0\_DQS\_DN\_11  
DDR0\_DQS\_DN\_10  
DDR0\_DQS\_DN\_9  
DDR0\_DQS\_DN\_8  
DDR0\_DQS\_DN\_7  
DDR0\_DQS\_DN\_6  
DDR0\_DQS\_DN\_5  
DDR0\_DQS\_DN\_4  
DDR0\_DQS\_DN\_3  
DDR0\_DQS\_DN\_2  
DDR0\_DQS\_DN\_1  
DDR0\_DQS\_DN\_0

DDR0\_MA\_15  
DDR0\_MA\_14  
DDR0\_MA\_13  
DDR0\_MA\_12  
DDR0\_MA\_11  
DDR0\_MA\_10  
DDR0\_MA\_9  
DDR0\_MA\_8  
DDR0\_MA\_7  
DDR0\_MA\_6  
DDR0\_MA\_5  
DDR0\_MA\_4  
DDR0\_MA\_3  
DDR0\_MA\_2  
DDR0\_MA\_1  
DDR0\_MA\_0

DDR0\_ECC\_7  
DDR0\_ECC\_6  
DDR0\_ECC\_5  
DDR0\_ECC\_4  
DDR0\_ECC\_3  
DDR0\_ECC\_2  
DDR0\_ECC\_1  
DDR0\_ECC\_0

DDR0\_CKE\_5  
DDR0\_CKE\_4  
DDR0\_CKE\_3  
DDR0\_CKE\_2  
DDR0\_CKE\_1  
DDR0\_CKE\_0

DDR0\_BA\_2  
DDR0\_BA\_1  
DDR0\_BA\_0  
DDR0\_ODT\_5  
DDR0\_ODT\_4  
DDR0\_ODT\_3  
DDR0\_ODT\_2  
DDR0\_ODT\_1  
DDR0\_ODT\_0

DDR0\_WE\_N  
DDR0\_RAS\_N  
DDR0\_PARR\_N  
DDR0\_CAS\_N  
DDR0\_MA\_PAR

CPU2 M.CH0 DQS 17 DP  
CPU2 M.CH0 DQS 16 DP  
CPU2 M.CH0 DQS 15 DP  
CPU2 M.CH0 DQS 14 DP  
CPU2 M.CH0 DQS 13 DP  
CPU2 M.CH0 DQS 12 DP  
CPU2 M.CH0 DQS 11 DP  
CPU2 M.CH0 DQS 10 DP  
CPU2 M.CH0 DQS 9 DP  
CPU2 M.CH0 DQS 8 DP  
CPU2 M.CH0 DQS 7 DP  
CPU2 M.CH0 DQS 6 DP  
CPU2 M.CH0 DQS 5 DP  
CPU2 M.CH0 DQS 4 DP  
CPU2 M.CH0 DQS 3 DP  
CPU2 M.CH0 DQS 2 DP  
CPU2 M.CH0 DQS 1 DP  
CPU2 M.CH0 DQS 0 DP

CPU2 M.CH0 DQS 16 DN  
CPU2 M.CH0 DQS 15 DN  
CPU2 M.CH0 DQS 14 DN  
CPU2 M.CH0 DQS 13 DN  
CPU2 M.CH0 DQS 12 DN  
CPU2 M.CH0 DQS 11 DN  
CPU2 M.CH0 DQS 10 DN  
CPU2 M.CH0 DQS 9 DN  
CPU2 M.CH0 DQS 8 DN  
CPU2 M.CH0 DQS 7 DN  
CPU2 M.CH0 DQS 6 DN  
CPU2 M.CH0 DQS 5 DN  
CPU2 M.CH0 DQS 4 DN  
CPU2 M.CH0 DQS 3 DN  
CPU2 M.CH0 DQS 2 DN  
CPU2 M.CH0 DQS 1 DN  
CPU2 M.CH0 DQS 0 DN

CPU2 M.CH0 MA 15  
CPU2 M.CH0 MA 14  
CPU2 M.CH0 MA 13  
CPU2 M.CH0 MA 12  
CPU2 M.CH0 MA 11  
CPU2 M.CH0 MA 10  
CPU2 M.CH0 MA 9  
CPU2 M.CH0 MA 8  
CPU2 M.CH0 MA 7  
CPU2 M.CH0 MA 6  
CPU2 M.CH0 MA 5  
CPU2 M.CH0 MA 4  
CPU2 M.CH0 MA 3  
CPU2 M.CH0 MA 2  
CPU2 M.CH0 MA 1  
CPU2 M.CH0 MA 0

CPU2 M.CH0 ECC 7  
CPU2 M.CH0 ECC 6  
CPU2 M.CH0 ECC 5  
CPU2 M.CH0 ECC 4  
CPU2 M.CH0 ECC 3  
CPU2 M.CH0 ECC 2  
CPU2 M.CH0 ECC 1  
CPU2 M.CH0 ECC 0

CPU2 M.CH0 CKE 1  
CPU2 M.CH0 CKE 0  
CPU2 M.CH0 BA 2  
CPU2 M.CH0 BA 1  
CPU2 M.CH0 BA 0  
CPU2 M.CH0 ODT 1  
CPU2 M.CH0 ODT 0

CPU2 M.CH0 WE\_N  
CPU2 M.CH0 RAS\_N  
CPU2 M.CH0 PERR\_N  
CPU2 M.CH0 CAS\_N  
CPU2 M.CH0 MA\_PAR

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## DDR\_CH1

CPU2C

&lt;&lt;41&gt; CPU2\_M.CH1\_DQ\_[B3..0]

CPU2 M.CH1 DQ 63 DF40  
CPU2 M.CH1 DQ 62 DA39  
CPU2 M.CH1 DQ 61 DC37  
CPU2 M.CH1 DQ 60 DA37  
CPU2 M.CH1 DQ 59 DA39  
CPU2 M.CH1 DQ 58 DD40  
CPU2 M.CH1 DQ 57 DF38  
CPU2 M.CH1 DQ 56 DF38  
CPU2 M.CH1 DQ 55 CV40  
CPU2 M.CH1 DQ 54 CT40  
CPU2 M.CH1 DQ 53 CV40  
CPU2 M.CH1 DQ 52 CT36  
CPU2 M.CH1 DQ 51 CU41  
CPU2 M.CH1 DQ 50 CR41  
CPU2 M.CH1 DQ 49 CL37  
CPU2 M.CH1 DQ 48 CR37  
CPU2 M.CH1 DQ 47 DE35  
CPU2 M.CH1 DQ 46 DF34  
CPU2 M.CH1 DQ 45 CY32  
CPU2 M.CH1 DQ 44 DA31  
CPU2 M.CH1 DQ 43 DA35  
CPU2 M.CH1 DQ 42 DC35  
CPU2 M.CH1 DQ 41 DD32  
CPU2 M.CH1 DQ 40 DA33  
CPU2 M.CH1 DQ 39 CR33  
CPU2 M.CH1 DQ 38 CL33  
CPU2 M.CH1 DQ 37 CR29  
CPU2 M.CH1 DQ 36 CU29  
CPU2 M.CH1 DQ 35 CP34  
CPU2 M.CH1 DQ 34 CT34  
CPU2 M.CH1 DQ 33 CR32  
CPU2 M.CH1 DQ 32 CT30  
CPU2 M.CH1 DQ 31 CV16  
CPU2 M.CH1 DQ 30 CT16  
CPU2 M.CH1 DQ 29 CV12  
CPU2 M.CH1 DQ 28 CT12  
CPU2 M.CH1 DQ 27 CU17  
CPU2 M.CH1 DQ 26 CR17  
CPU2 M.CH1 DQ 25 CU13  
CPU2 M.CH1 DQ 24 CR13  
CPU2 M.CH1 DQ 23 CV10  
CPU2 M.CH1 DQ 22 CW9  
CPU2 M.CH1 DQ 21 CR6  
CPU2 M.CH1 DQ 20 CP10  
CPU2 M.CH1 DQ 19 CU10  
CPU2 M.CH1 DQ 18 CU7  
CPU2 M.CH1 DQ 17 CR7  
CPU2 M.CH1 DQ 16 DF10  
CPU2 M.CH1 DQ 15 DB10  
CPU2 M.CH1 DQ 14 DB6  
CPU2 M.CH1 DQ 13 CV6  
CPU2 M.CH1 DQ 12 DE11  
CPU2 M.CH1 DQ 11 DE11  
CPU2 M.CH1 DQ 10 DE11  
CPU2 M.CH1 DQ 9 DC7  
CPU2 M.CH1 DQ 8 DA7  
CPU2 M.CH1 DQ 7 CW3  
CPU2 M.CH1 DQ 6 CV2  
CPU2 M.CH1 DQ 5 CL3  
CPU2 M.CH1 DQ 4 CH4  
CPU2 M.CH1 DQ 3 CV4  
CPU2 M.CH1 DQ 2 CV4  
CPU2 M.CH1 DQ 1 CP2  
CPU2 M.CH1 DQ 0 CP4

DDR1 DQ 63  
DDR1 DQ 62  
DDR1 DQ 61  
DDR1 DQ 60  
DDR1 DQ 59  
DDR1 DQ 58  
DDR1 DQ 57  
DDR1 DQ 56  
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DDR1 DQ 8  
DDR1 DQ 7  
DDR1 DQ 6  
DDR1 DQ 5  
DDR1 DQ 4  
DDR1 DQ 3  
DDR1 DQ 2  
DDR1 DQ 1  
DDR1 DQ 0

CPU2 M.CH1 DQS 17 DP  
CPU2 M.CH1 DQS 16 DP  
CPU2 M.CH1 DQS 15 DP  
CPU2 M.CH1 DQS 14 DP  
CPU2 M.CH1 DQS 13 DP  
CPU2 M.CH1 DQS 12 DP  
CPU2 M.CH1 DQS 11 DP  
CPU2 M.CH1 DQS 10 DP  
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CPU2 M.CH1 DQS 7 DP  
CPU2 M.CH1 DQS 6 DP  
CPU2 M.CH1 DQS 5 DP  
CPU2 M.CH1 DQS 4 DP  
CPU2 M.CH1 DQS 3 DP  
CPU2 M.CH1 DQS 2 DP  
CPU2 M.CH1 DQS 1 DP  
CPU2 M.CH1 DQS 0 DP

CPU2 M.CH1 DQS 16 DN  
CPU2 M.CH1 DQS 15 DN  
CPU2 M.CH1 DQS 14 DN  
CPU2 M.CH1 DQS 13 DN  
CPU2 M.CH1 DQS 12 DN  
CPU2 M.CH1 DQS 11 DN  
CPU2 M.CH1 DQS 10 DN  
CPU2 M.CH1 DQS 9 DN  
CPU2 M.CH1 DQS 8 DN  
CPU2 M.CH1 DQS 7 DN  
CPU2 M.CH1 DQS 6 DN  
CPU2 M.CH1 DQS 5 DN  
CPU2 M.CH1 DQS 4 DN  
CPU2 M.CH1 DQS 3 DN  
CPU2 M.CH1 DQS 2 DN  
CPU2 M.CH1 DQS 1 DN  
CPU2 M.CH1 DQS 0 DN

CPU2 M.CH1 MA 15  
CPU2 M.CH1 MA 14  
CPU2 M.CH1 MA 13  
CPU2 M.CH1 MA 12  
CPU2 M.CH1 MA 11  
CPU2 M.CH1 MA 10  
CPU2 M.CH1 MA 9  
CPU2 M.CH1 MA 8  
CPU2 M.CH1 MA 7  
CPU2 M.CH1 MA 6  
CPU2 M.CH1 MA 5  
CPU2 M.CH1 MA 4  
CPU2 M.CH1 MA 3  
CPU2 M.CH1 MA 2  
CPU2 M.CH1 MA 1  
CPU2 M.CH1 MA 0

CPU2 M.CH1 ECC 7  
CPU2 M.CH1 ECC 6  
CPU2 M.CH1 ECC 5  
CPU2 M.CH1 ECC 4  
CPU2 M.CH1 ECC 3  
CPU2 M.CH1 ECC 2  
CPU2 M.CH1 ECC 1  
CPU2 M.CH1 ECC 0

CPU2 M.CH1 CKE 1  
CPU2 M.CH1 CKE 0  
CPU2 M.CH1 BA 2  
CPU2 M.CH1 BA 1  
CPU2 M.CH1 BA 0  
CPU2 M.CH1 ODT 1  
CPU2 M.CH1 ODT 0

CPU2 M.CH1 WE\_N  
CPU2 M.CH1 RAS\_N  
CPU2 M.CH1 PERR\_N  
CPU2 M.CH1 CAS\_N  
CPU2 M.CH1 MA\_PAR

RoseCity-PG35

RoseCity-PG36

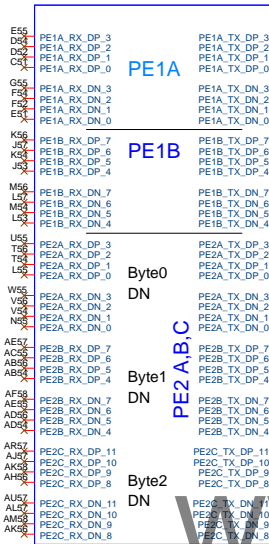
Title  
SCHEM, PWA, LITTLE, SURDWG NO  
PN27HRev  
A01

Date: Wednesday, June 20, 2012 Sheet 32 of 96

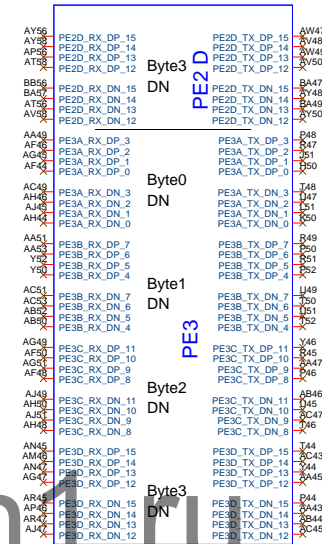




# CPU2F



# CPU2G



SandyBridge\_EPEX\_EDS\_Vol1\_26601.0.5.pvd Figure 1-3 pg.16

Port0	Port1	Port2	Port3
DMI	PE1[A:B]	PE2[A:B:C:D]	PE3[A:B:C:D]
IOU2---IOU2		IOU0	IOU1
Unused	Unused	X16 slot	X16 slot

## QPI0 interface

CPU2I

Lane Reversed &  
DP/IDN swapped  
on most lanes  
for routing

<15> QPI_CPU1_CPU2_P1P0_00_DN	<15> QPI_CPU1_CPU2_P1P0_01_DN	<15> QPI_CPU1_CPU2_P1P0_02_DN	<15> QPI_CPU1_CPU2_P1P0_03_DN	<15> QPI_CPU1_CPU2_P1P0_04_DN	<15> QPI_CPU1_CPU2_P1P0_05_DN	<15> QPI_CPU1_CPU2_P1P0_06_DN	<15> QPI_CPU1_CPU2_P1P0_07_DP	<15> QPI_CPU1_CPU2_P1P0_08_DN	<15> QPI_CPU1_CPU2_P1P0_09_DP	<15> QPI_CPU1_CPU2_P1P0_10_DN	<15> QPI_CPU1_CPU2_P1P0_11_DN	<15> QPI_CPU1_CPU2_P1P0_12_DN	<15> QPI_CPU1_CPU2_P1P0_13_DN	<15> QPI_CPU1_CPU2_P1P0_14_DN	<15> QPI_CPU1_CPU2_P1P0_15_DN	<15> QPI_CPU1_CPU2_P1P0_16_DN	<15> QPI_CPU1_CPU2_P1P0_17_DN	<15> QPI_CPU1_CPU2_P1P0_18_DN	<15> QPI_CPU1_CPU2_P1P0_19_DN
<15> QPI_CPU1_CPU2_P1P0_00_DP	<15> QPI_CPU1_CPU2_P1P0_01_DP	<15> QPI_CPU1_CPU2_P1P0_02_DP	<15> QPI_CPU1_CPU2_P1P0_03_DP	<15> QPI_CPU1_CPU2_P1P0_04_DP	<15> QPI_CPU1_CPU2_P1P0_05_DP	<15> QPI_CPU1_CPU2_P1P0_06_DP	<15> QPI_CPU1_CPU2_P1P0_07_DP	<15> QPI_CPU1_CPU2_P1P0_08_DP	<15> QPI_CPU1_CPU2_P1P0_09_DP	<15> QPI_CPU1_CPU2_P1P0_10_DP	<15> QPI_CPU1_CPU2_P1P0_11_DP	<15> QPI_CPU1_CPU2_P1P0_12_DP	<15> QPI_CPU1_CPU2_P1P0_13_DP	<15> QPI_CPU1_CPU2_P1P0_14_DP	<15> QPI_CPU1_CPU2_P1P0_15_DP	<15> QPI_CPU1_CPU2_P1P0_16_DP	<15> QPI_CPU1_CPU2_P1P0_17_DP	<15> QPI_CPU1_CPU2_P1P0_18_DP	<15> QPI_CPU1_CPU2_P1P0_19_DP

## QPI1 interface

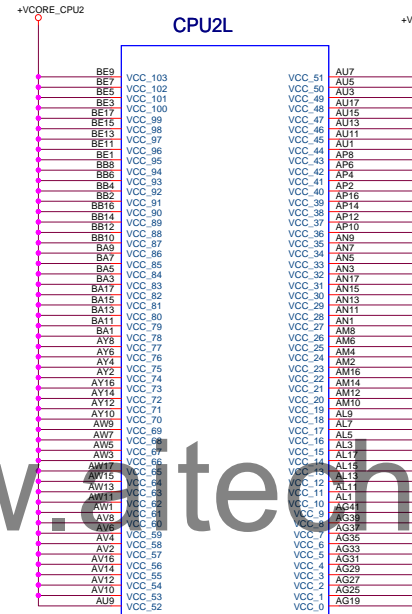
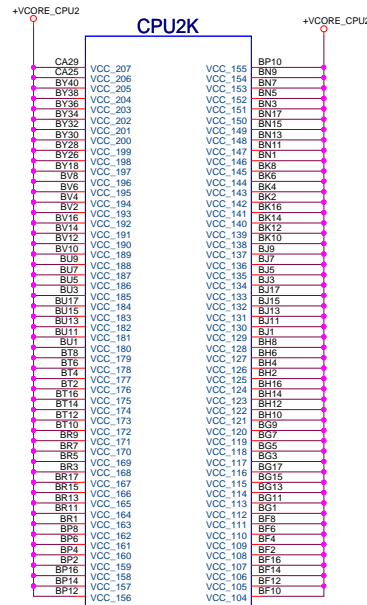
CPU2J

Lane Reversed &  
DP/IDN swapped  
on most lanes  
for routing

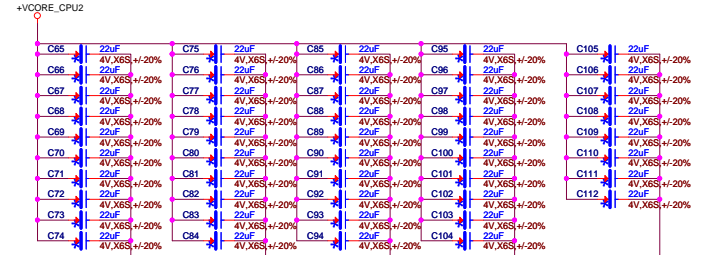
<15> QPI_CPU1_CPU2_P0P1_19_DP	<15> QPI_CPU1_CPU2_P0P1_18_DP	<15> QPI_CPU1_CPU2_P0P1_17_DP	<15> QPI_CPU1_CPU2_P0P1_16_DP	<15> QPI_CPU1_CPU2_P0P1_15_DP	<15> QPI_CPU1_CPU2_P0P1_14_DP	<15> QPI_CPU1_CPU2_P0P1_13_DP	<15> QPI_CPU1_CPU2_P0P1_12_DP	<15> QPI_CPU1_CPU2_P0P1_11_DP	<15> QPI_CPU1_CPU2_P0P1_10_DP	<15> QPI_CPU1_CPU2_P0P1_09_DP	<15> QPI_CPU1_CPU2_P0P1_08_DP	<15> QPI_CPU1_CPU2_P0P1_07_DP	<15> QPI_CPU1_CPU2_P0P1_06_DP	<15> QPI_CPU1_CPU2_P0P1_05_DP	<15> QPI_CPU1_CPU2_P0P1_04_DP	<15> QPI_CPU1_CPU2_P0P1_03_DP	<15> QPI_CPU1_CPU2_P0P1_02_DP	<15> QPI_CPU1_CPU2_P0P1_01_DP	<15> QPI_CPU1_CPU2_P0P1_00_DP
<15> QPI_CPU1_CPU2_P0P1_19_DN	<15> QPI_CPU1_CPU2_P0P1_18_DN	<15> QPI_CPU1_CPU2_P0P1_17_DN	<15> QPI_CPU1_CPU2_P0P1_16_DN	<15> QPI_CPU1_CPU2_P0P1_15_DN	<15> QPI_CPU1_CPU2_P0P1_14_DN	<15> QPI_CPU1_CPU2_P0P1_13_DN	<15> QPI_CPU1_CPU2_P0P1_12_DN	<15> QPI_CPU1_CPU2_P0P1_11_DN	<15> QPI_CPU1_CPU2_P0P1_10_DN	<15> QPI_CPU1_CPU2_P0P1_09_DN	<15> QPI_CPU1_CPU2_P0P1_08_DN	<15> QPI_CPU1_CPU2_P0P1_07_DN	<15> QPI_CPU1_CPU2_P0P1_06_DN	<15> QPI_CPU1_CPU2_P0P1_05_DN	<15> QPI_CPU1_CPU2_P0P1_04_DN	<15> QPI_CPU1_CPU2_P0P1_03_DN	<15> QPI_CPU1_CPU2_P0P1_02_DN	<15> QPI_CPU1_CPU2_P0P1_01_DN	<15> QPI_CPU1_CPU2_P0P1_00_DN

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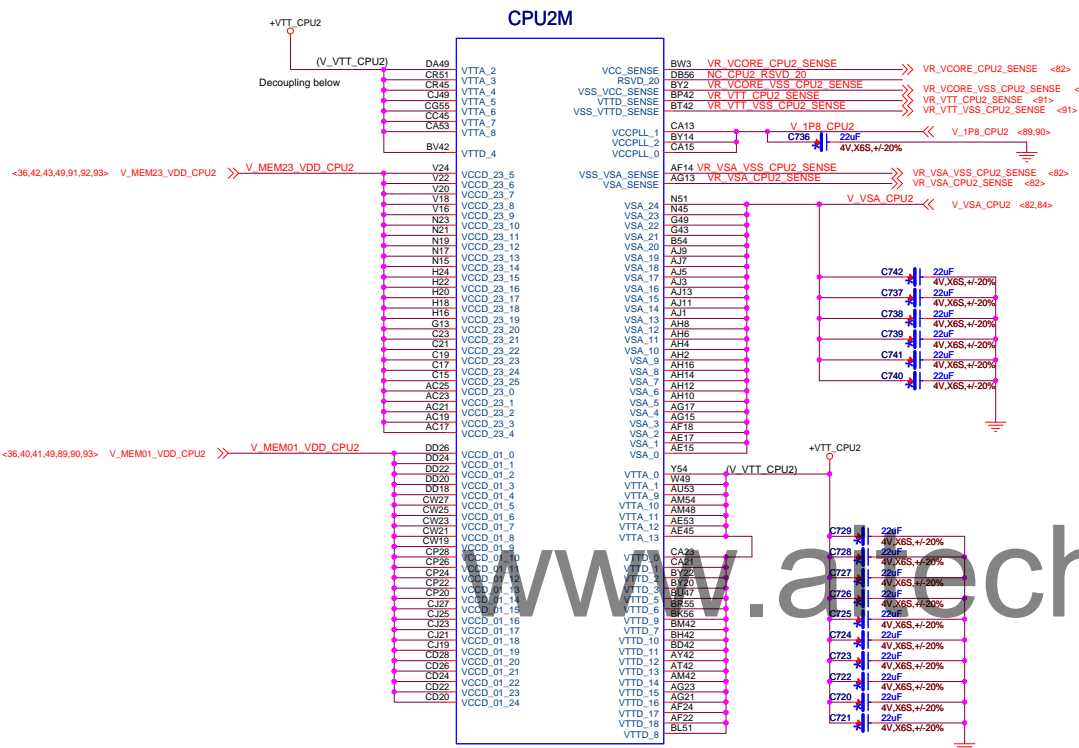




Hight Temp X6S Caps. Place in CPU cavity



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RoseCity-PG45



## CPU2N

CY40	VSS_547	N9
AW55	VSS_546	N5
AG43	VSS_545	N4
CW51	VSS_544	N3
C3	VSS_543	N2
D2	VSS_542	N1
D5	VSS_541	N0
DC3	VSS_540	N0
E1	VSS_539	N0
V46	VSS_538	N0
BK47	VSS_537	N0
BK50	VSS_536	N0
AL51	VSS_535	N0
V56	VSS_534	N0
Y42	VSS_533	N0
Y40	VSS_532	N0
Y38	VSS_531	N0
Y32	VSS_530	N0
Y30	VSS_529	N0
Y28	VSS_528	N0
Y12	VSS_527	N0
Y10	VSS_526	N0
W5	VSS_525	N0
W53	VSS_524	N0
W51	VSS_523	N0
W5	VSS_522	N0
W47	VSS_521	N0
W45	VSS_520	N0
W43	VSS_519	N0
W41	VSS_518	N0
W37	VSS_517	N0
W35	VSS_516	N0
W13	VSS_515	N0
V8	VSS_514	N0
V50	VSS_513	N0
V48	VSS_512	N0
V44	VSS_511	N0
V42	VSS_510	N0
V36	VSS_509	N0
V34	VSS_508	N0
V28	VSS_507	N0
V26	VSS_506	N0
V5	VSS_505	N0
U5	VSS_504	N0
T8	VSS_503	N0
T6	VSS_502	N0
T4	VSS_501	N0
T2	VSS_500	N0
R7	VSS_499	N0
R55	VSS_497	N0
R5	VSS_496	N0
R39	VSS_495	N0
R35	VSS_494	N0
R31	VSS_493	N0
R3	VSS_492	N0
R11	VSS_491	N0
R29	VSS_490	N0
P54	VSS_489	N0
P6	VSS_488	N0
P54	VSS_487	N0
P40	VSS_486	N0
P38	VSS_485	N0
P32	VSS_484	N0
P30	VSS_483	N0
P26	VSS_482	N0
P14	VSS_481	N0
P12	VSS_480	N0
P10	VSS_479	N0
	VSS_478	N0

## CPU2O

E31	VSS_409	E34
E29	VSS_408	E32
E27	VSS_407	E30
DF52	VSS_406	DF52
DF50	VSS_405	DF50
DF48	VSS_404	DF48
DF46	VSS_403	DF46
DF44	VSS_402	DF44
DF42	VSS_401	DF42
DF36	VSS_400	DF36
DF34	VSS_399	DF34
DF12	VSS_398	DF12
DE1	VSS_397	DE1
DE53	VSS_396	DE53
DE41	VSS_395	DE41
DD6	VSS_394	DD6
DD38	VSS_393	DD38
DD36	VSS_392	DD36
DD34	VSS_391	DD34
DD12	VSS_390	DD12
DD10	VSS_389	DD10
DC5	VSS_388	DC5
DC41	VSS_387	DC41
DB58	VSS_386	DB58
DB36	VSS_385	DB36
DB34	VSS_384	DB34
DB32	VSS_383	DB32
DB30	VSS_382	DB30
DA9	VSS_381	DA9
DA51	VSS_380	DA51
DA3	VSS_379	DA3
DA47	VSS_378	DA47
DA45	VSS_377	DA45
DA43	VSS_376	DA43
DA41	VSS_375	DA41
DA3	VSS_374	DA3
DA11	VSS_373	DA11
D8	VSS_372	D8
D36	VSS_371	D36
D26	VSS_370	D26
CY8	VSS_369	CY8
CY2	VSS_368	CY2
CY40	VSS_367	CY40
CY36	VSS_366	CY36
CY2	VSS_365	CY2
CY16	VSS_364	CY16
CY12	VSS_363	CY12
CY10	VSS_362	CY10
CW7	VSS_361	CW7
CW57	VSS_360	CW57
CW55	VSS_359	CW55
CW53	VSS_358	CW53
CW5	VSS_357	CW5
CW35	VSS_356	CW35
CW33	VSS_355	CW33
CW31	VSS_354	CW31
CW27	VSS_353	CW27
CW25	VSS_352	CW25
CW23	VSS_351	CW23
CW21	VSS_350	CW21
CW19	VSS_349	CW19
CW17	VSS_348	CW17
CW15	VSS_347	CW15
CW13	VSS_346	CW13
CW11	VSS_345	CW11
CW9	VSS_344	CW9
CW7	VSS_343	CW7
CW5	VSS_342	CW5

## CPU2P

CJ29	VSS_273	C55
CJ17	VSS_272	C53
CJ15	VSS_271	C51
CJ13	VSS_270	C49
CJ11	VSS_269	C47
CH6	VSS_268	CH6
CH50	VSS_267	CH50
CH48	VSS_266	CH48
CH46	VSS_265	CH46
CH44	VSS_264	CH44
CH42	VSS_263	CH42
CH40	VSS_262	CH40
CH38	VSS_261	CH38
CH36	VSS_260	CH36
CH34	VSS_259	CH34
CH32	VSS_258	CH32
CH30	VSS_257	CH30
CH28	VSS_256	CH28
CH26	VSS_255	CH26
CH24	VSS_254	CH24
CH22	VSS_253	CH22
CH20	VSS_252	CH20
CH18	VSS_251	CH18
CH16	VSS_250	CH16
CH14	VSS_249	CH14
CH12	VSS_248	CH12
CH10	VSS_247	CH10
CH8	VSS_246	CH8
CH6	VSS_245	CH6
CH4	VSS_244	CH4
CH2	VSS_243	CH2
CH0	VSS_242	CH0
CH12	VSS_241	CH12
CH10	VSS_240	CH10
CH8	VSS_239	CH8
CH6	VSS_238	CH6
CH4	VSS_237	CH4
CH2	VSS_236	CH2
CH0	VSS_235	CH0
CH18	VSS_234	CH18
CH16	VSS_233	CH16
CH14	VSS_232	CH14
CH12	VSS_231	CH12
CH10	VSS_230	CH10
CH8	VSS_229	CH8
CH6	VSS_228	CH6
CH4	VSS_227	CH4
CH2	VSS_226	CH2
CH0	VSS_225	CH0
CH18	VSS_224	CH18
CH16	VSS_223	CH16
CH14	VSS_222	CH14
CH12	VSS_221	CH12
CH10	VSS_220	CH10
CH8	VSS_219	CH8
CH6	VSS_218	CH6
CH4	VSS_217	CH4
CH2	VSS_216	CH2
CH0	VSS_215	CH0
CH18	VSS_214	CH18
CH16	VSS_213	CH16
CH14	VSS_212	CH14
CH12	VSS_211	CH12
CH10	VSS_210	CH10
CH8	VSS_209	CH8
CH6	VSS_208	CH6
CH4	VSS_207	CH4
CH2	VSS_206	CH2

## CPU2Q

BD16	VSS_136	AK46
BD14	VSS_135	AK44
BD12	VSS_134	AK42
BD10	VSS_133	AK40
BD8	VSS_132	AK38
BD6	VSS_131	AK36
BD4	VSS_130	AK34
BD2	VSS_129	AK32
BD0	VSS_128	AK30
BD16	VSS_127	AK28
BD14	VSS_126	AK26
BD12	VSS_125	AK24
BD10	VSS_124	AK22
BD8	VSS_123	AK20
BD6	VSS_122	AK18
BD4	VSS_121	AK16
BD2	VSS_120	AK14
BD0	VSS_119	AK12
BD16	VSS_118	AK10
BD14	VSS_117	AK08
BD12	VSS_116	AK06
BD10	VSS_115	AK04
BD8	VSS_114	AK02
BD6	VSS_113	AK00
BD4	VSS_112	AK00
BD2	VSS_111	AK00
BD0	VSS_110	AK00
BD16	VSS_109	AK00
BD14	VSS_108	AK00
BD12	VSS_107	AK00
BD10	VSS_106	AK00
BD8	VSS_105	AK00
BD6	VSS_104	AK00
BD4	VSS_103	AK00
BD2	VSS_102	AK00
BD0	VSS_101	AK00
BD16	VSS_100	AK00
BD14	VSS_99	AK00
BD12	VSS_98	AK00
BD10	VSS_97	AK00
BD8	VSS_96	AK00
BD6	VSS_95	AK00
BD4	VSS_94	AK00
BD2	VSS_93	AK00
BD0	VSS_92	AK00
BD16	VSS_91	AK00
BD14	VSS_90	AK00
BD12	VSS_89	AK00
BD10	VSS_88	AK00
BD8	VSS_87	AK00
BD6	VSS_86	AK00
BD4	VSS_85	AK00
BD2	VSS_84	AK00
BD0	VSS_83	AK00
BD16	VSS_82	AK00
BD14	VSS_81	AK00
BD12	VSS_80	AK00
BD10	VSS_79	AK00
BD8	VSS_78	AK00
BD6	VSS_77	AK00
BD4	VSS_76	AK00
BD2	VSS_75	AK00
BD0	VSS_74	AK00
BD16	VSS_73	AK00
BD14	VSS_72	AK00
BD12	VSS_71	AK00
BD10	VSS_70	AK00
BD8	VSS_69	AK00



Title  
SCHEM, PWA, LITTLE, SUR

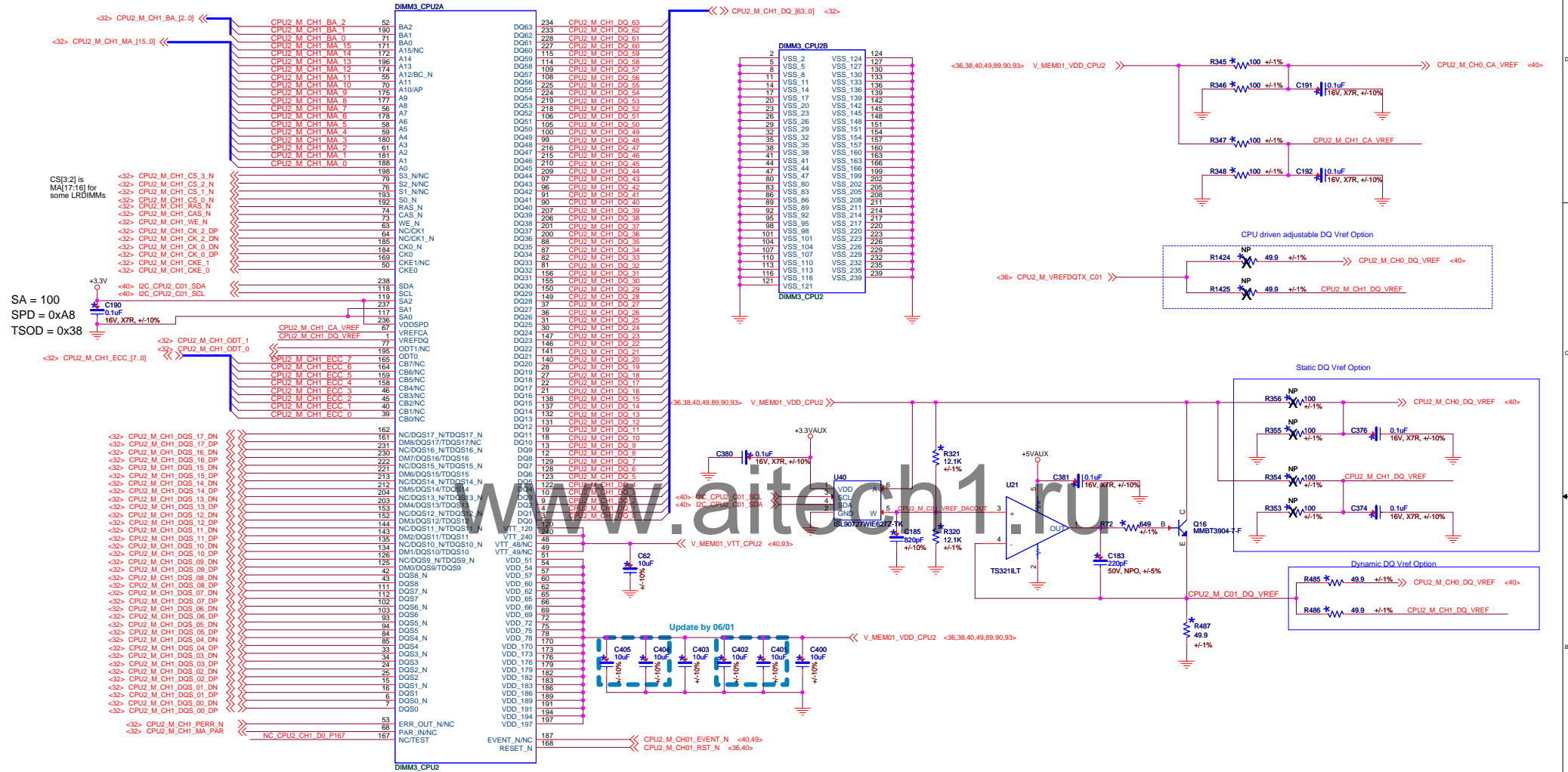
DWG NO  
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## CPU2\_CH1\_D0



### VC Testing

CPU2\_M\_CH1\_CA\_VREF

CPU2 M CH1 DQ VREF

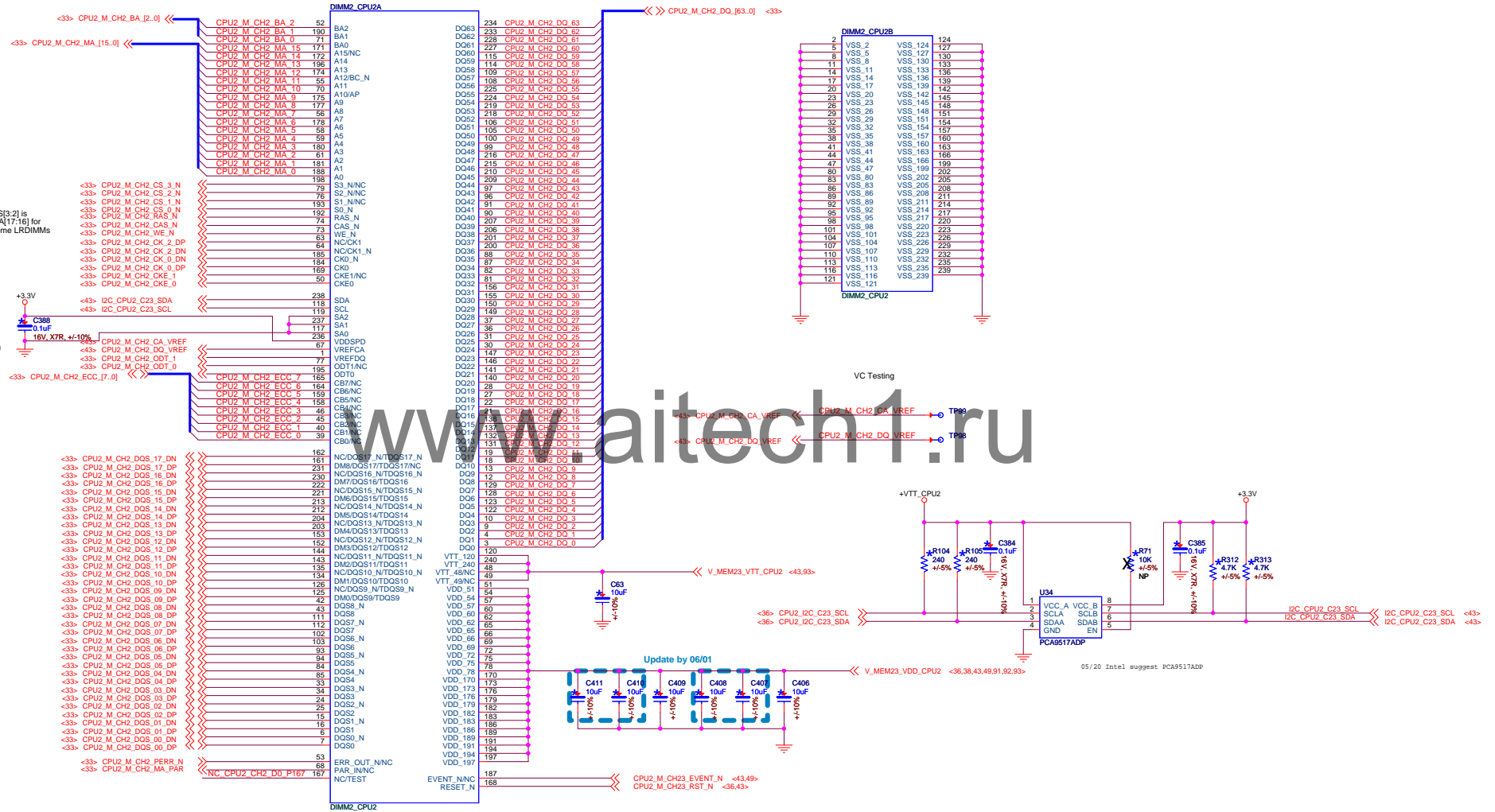


Title  
**SCHEM, PWA, LITTLE, SUR**

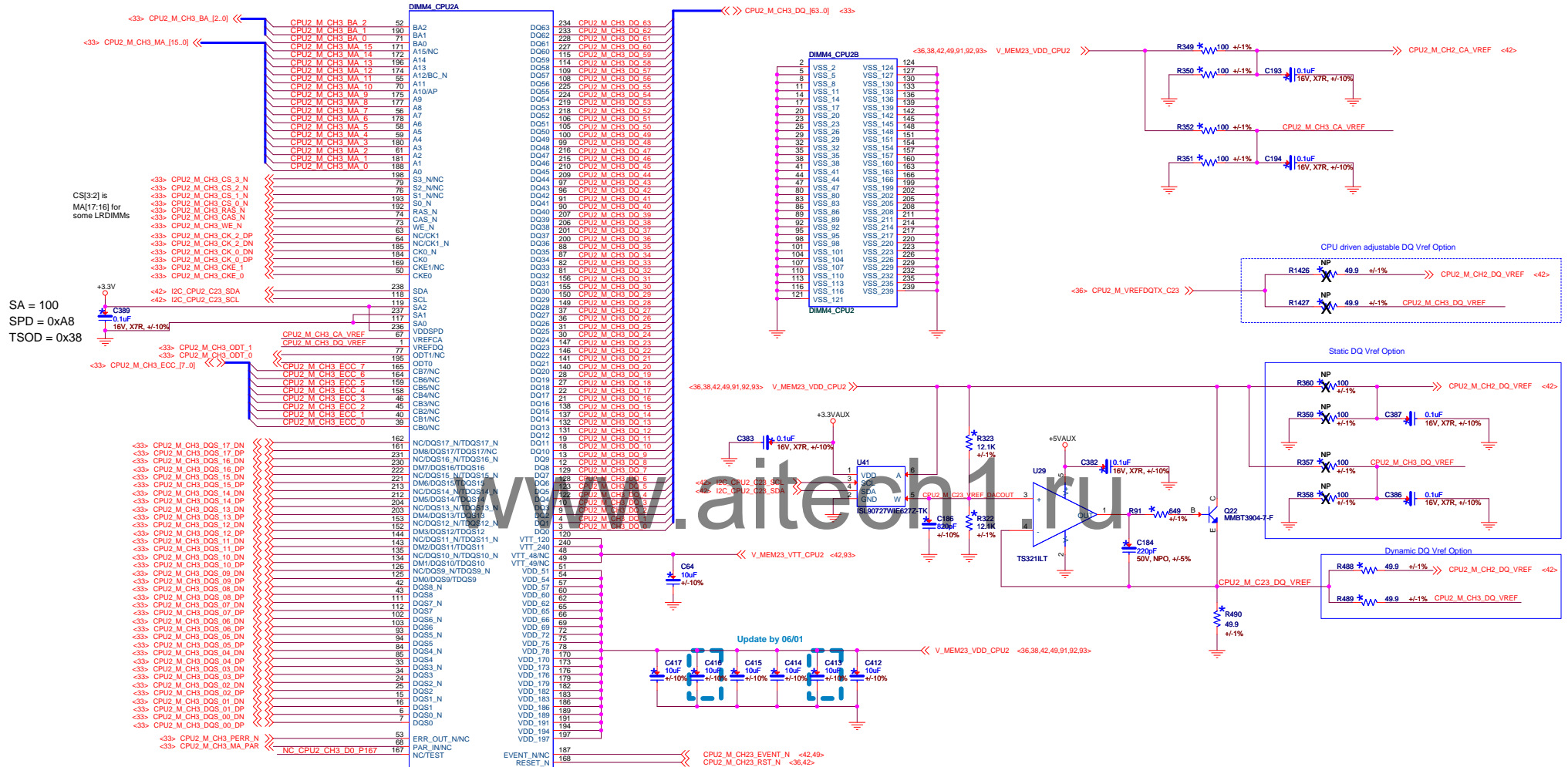
**PN27H**

A01

# CPU2\_CH2\_D0



## CPU2\_CH3\_D0



### VC Testing

CPU2 M CH3 CA VREF TP101

CPU2 M CH3 DQ VREF TP100



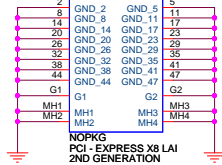
Title  
**SCHEM, PWA, LITTLE, SUR**

**PN27H**

A01

## LAI\_DMI\_PCIE

PE3_CPU1_1A_SB_3_DP	4	C1P_DA	C0P_DA	1	PE3_CPU1_1A_NB_3_DP
PE3_CPU1_1A_SB_3_DN	6	C1N_DA	C0N_DA	3	PE3_CPU1_1A_NB_3_DN
PE3_CPU1_1A_SB_2_DP	10	C3P_DA	C2P_DA	7	PE3_CPU1_1A_NB_2_DP
PE3_CPU1_1A_SB_2_DN	12	C3N_DA	C2N_DA	9	PE3_CPU1_1A_NB_2_DN
PE3_CPU1_1A_SB_1_DP	16	C5P_DA	C4P_DA	13	PE3_CPU1_1A_NB_1_DP
PE3_CPU1_1A_SB_1_DN	18	C5N_DA	C4N_DA	15	PE3_CPU1_1A_NB_1_DN
PE3_CPU1_1A_SB_0_DP	22	C7P_DA	C6P_DA	19	PE3_CPU1_1A_NB_0_DP
PE3_CPU1_1A_SB_0_DN	24	C7N_DA	C6N_DA	21	PE3_CPU1_1A_NB_0_DN
PE2_CPU1_DMI_SB_0_DP	28	C1P_DB	C0P_DB	25	PE2_CPU1_DMI_NB_0_DP
PE2_CPU1_DMI_SB_0_DN	30	C1N_DB	C0N_DB	27	PE2_CPU1_DMI_NB_0_DN
PE2_CPU1_DMI_SB_1_DP	34	C3P_DB	C2P_DB	31	PE2_CPU1_DMI_NB_1_DP
PE2_CPU1_DMI_SB_1_DN	36	C3N_DB	C2N_DB	33	PE2_CPU1_DMI_NB_1_DN
PE2_CPU1_DMI_SB_2_DP	40	C5P_DB	C4P_DB	37	PE2_CPU1_DMI_NB_2_DP
PE2_CPU1_DMI_SB_2_DN	42	C5N_DB	C4N_DB	39	PE2_CPU1_DMI_NB_2_DN
PE2_CPU1_DMI_SB_3_DP	46	C7P_DB	C6P_DB	43	PE2_CPU1_DMI_NB_3_DP
PE2_CPU1_DMI_SB_3_DN	48	C7N_DB	C6N_DB	45	PE2_CPU1_DMI_NB_3_DN



On SandyBridge side caps. Verify w/SI & layout

PCIe x4 Uplink port on CPU1/PCH

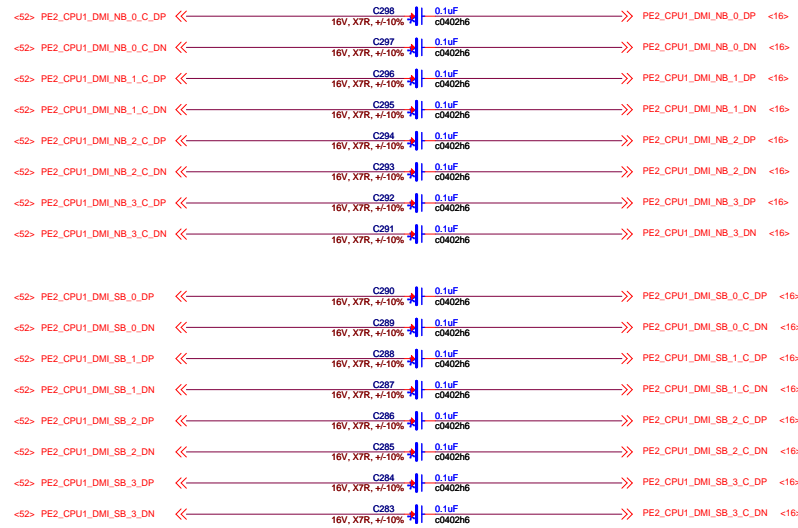
See Romley\_PDG\_Vol2\_27178,0.5.pvd Table 14-28

Polarity (DP/DN) may be swapped.

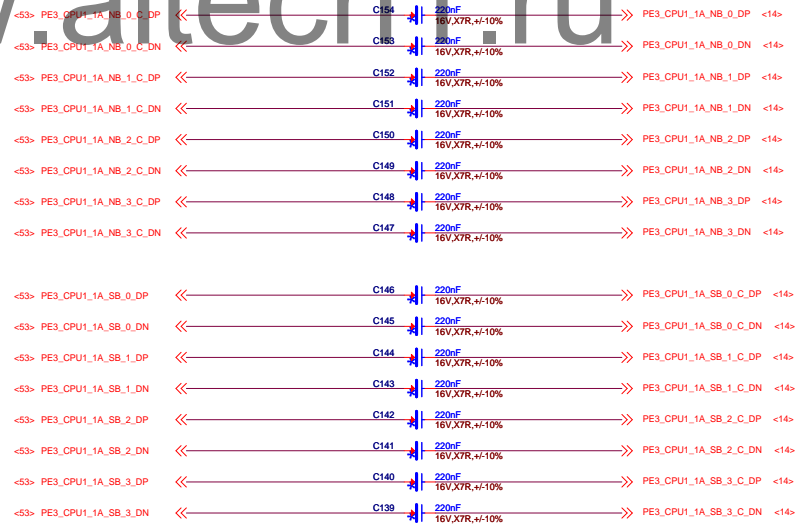
Entire link assignment may be reversed:

SB\_0 --> SB\_3  
SB\_1 --> SB\_2  
SB\_2 --> SB\_1  
SB\_3 --> SB\_0

## To DMI on PCH



## To X4 on PCH



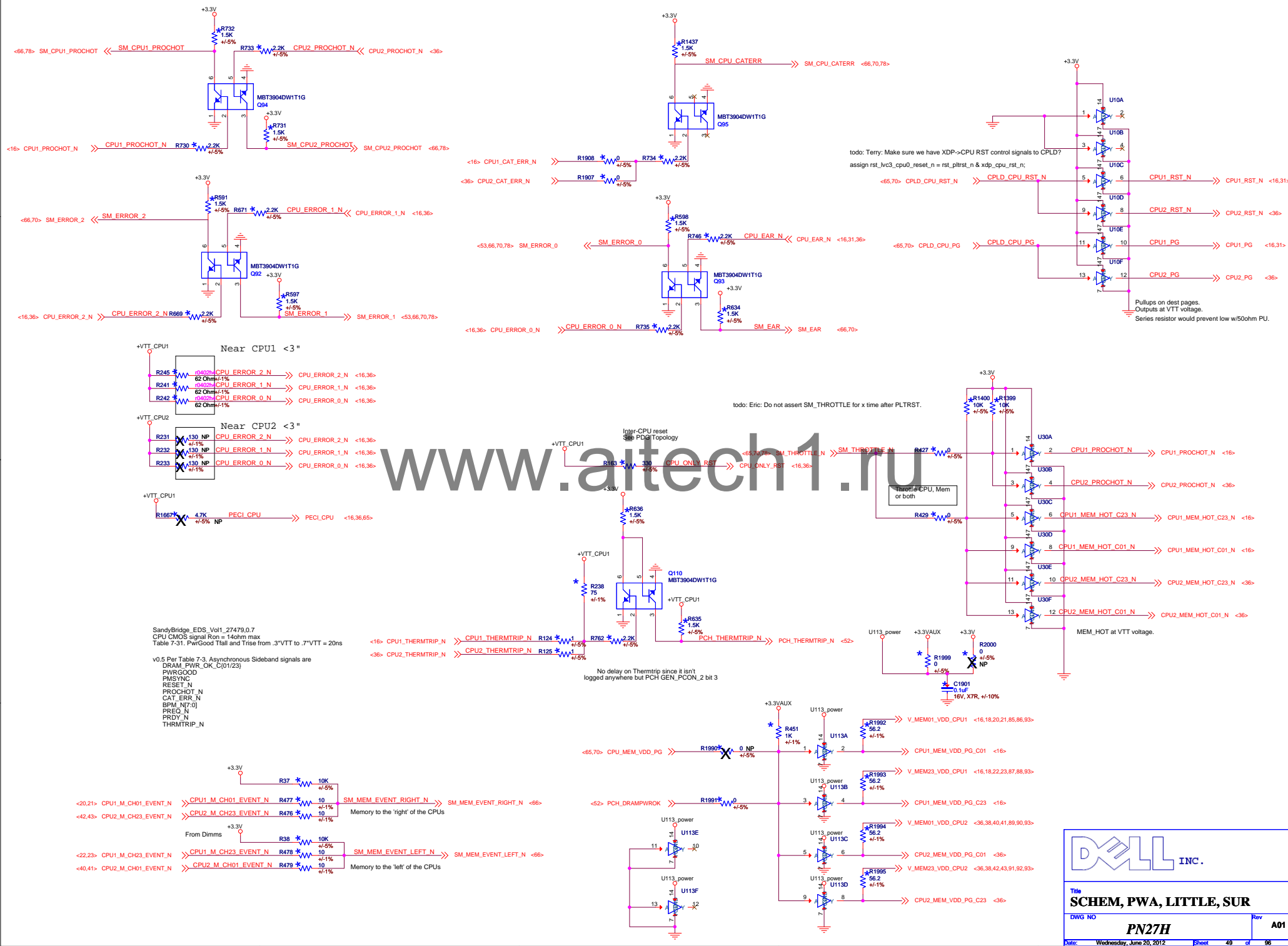
Title:  
**SCHEM, PWA, LITTLE, SUR**

DWG NO


**PN27H**

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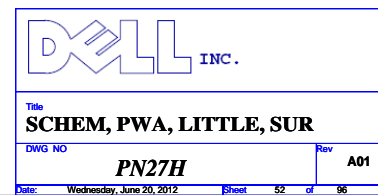
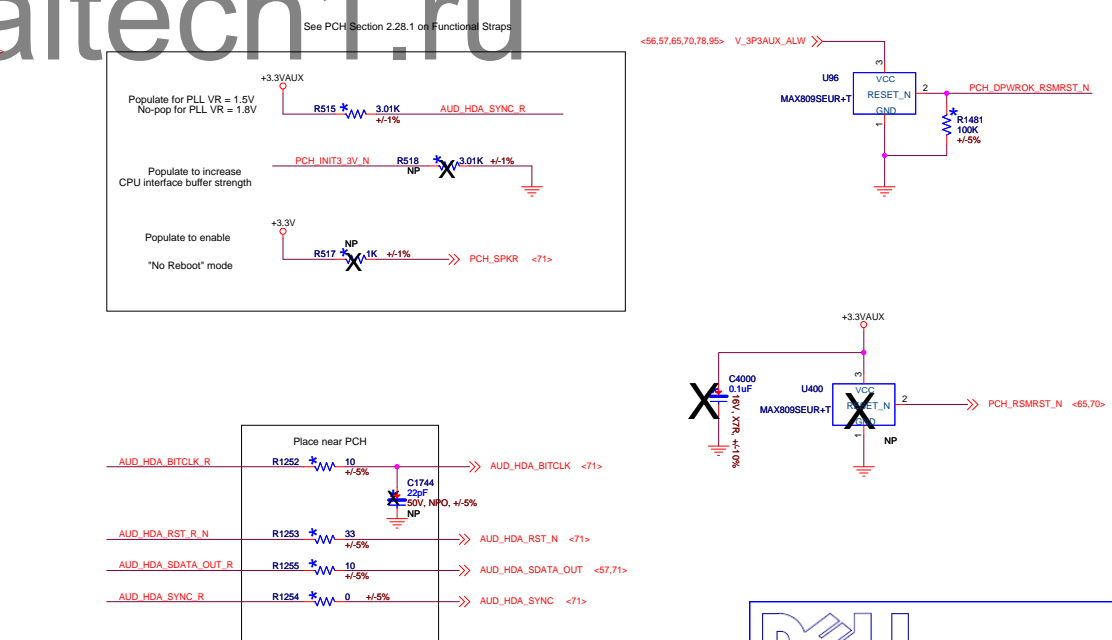
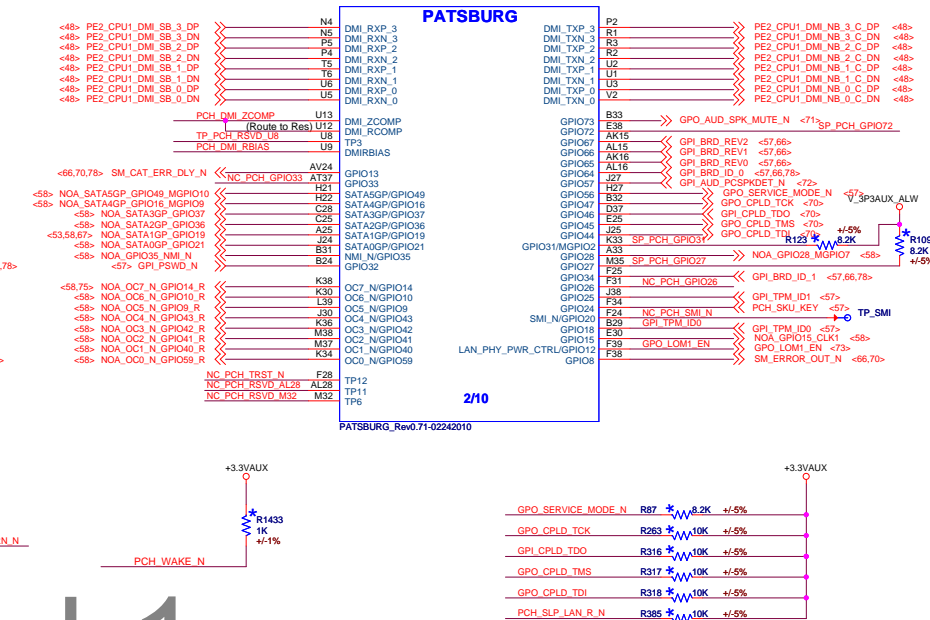
	
Title <b>SCHEM, PWA, LITTLE, SUR</b>	
DWG NO <b>PN27H</b>	Rev <b>A01</b>
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Title <b>SCHEM, PWA, LITTLE, SUR</b>	
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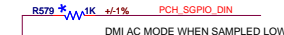
U\_PCH



## PATSBURG



PEG0 RBIA Sn/p			
Via spacing (center to center)	Trace spacing (edge to edge)	Trace coupling length	Decoupling Cap?
>=50mil (or, no via)	>=5h (stripline) >=7h (microstrip)	<=0.3"	No Cap



BOOT BIOS STRAPS		
DEFAULT 1,1: Weak PCH Internal PU		
PCH_SGPIO_DOUT	SATA1GP_GPIO19	
0	0	LPC
0	1	NAND
1	0	PCI
1	1	SPI

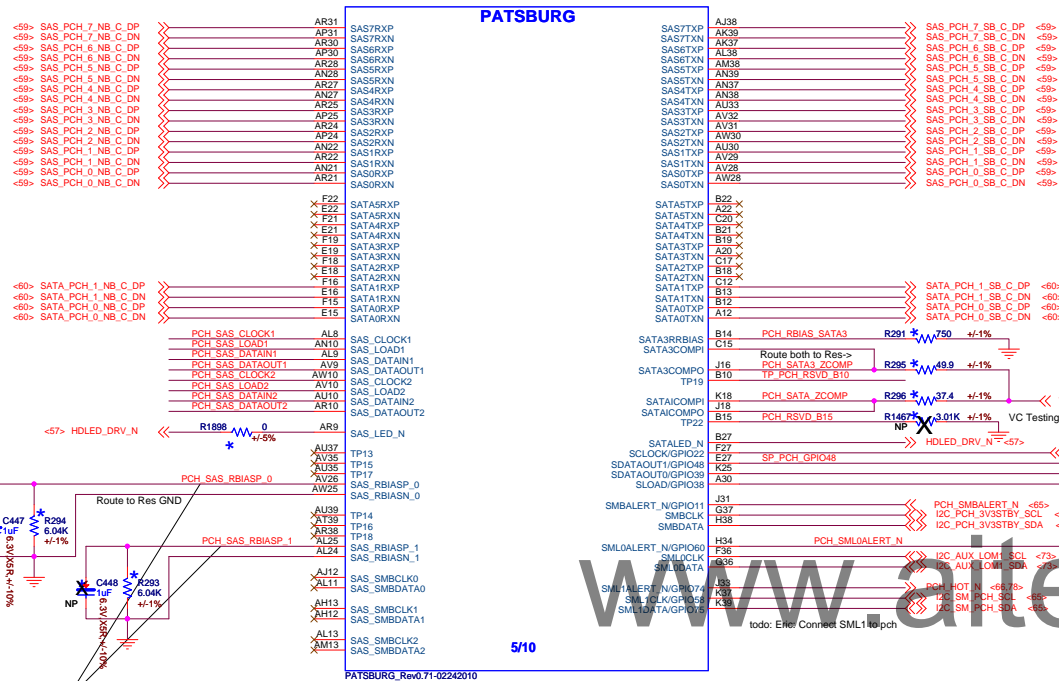
The diagram illustrates the connection of two boot bios straps, R577 and R578, to the NP (Not Present) pin. Both resistors are 1K with a +/-1% tolerance. R577 is connected to PCH\_SGPIO\_DOUT, and R578 is connected to NOA\_SATA1GP\_GPIO19. The diagram also shows the connection to the PCH\_SGPIO\_DOUT and NOA\_SATA1GP\_GPIO19 pins.



**PN27H**

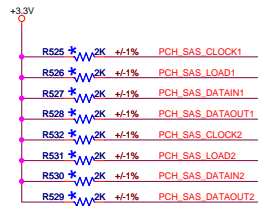
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U\_PCH



Via spacing (center to center)	Trace spacing (edge to edge)	Trace coupling length	Decoupling Cap?
>=26mil	>=3h (stripline) >=5h (microstrip)	<=0.3"	1uF/decap Required

SGPIO Pull Ups pg. 88  
Place PU within 2" from

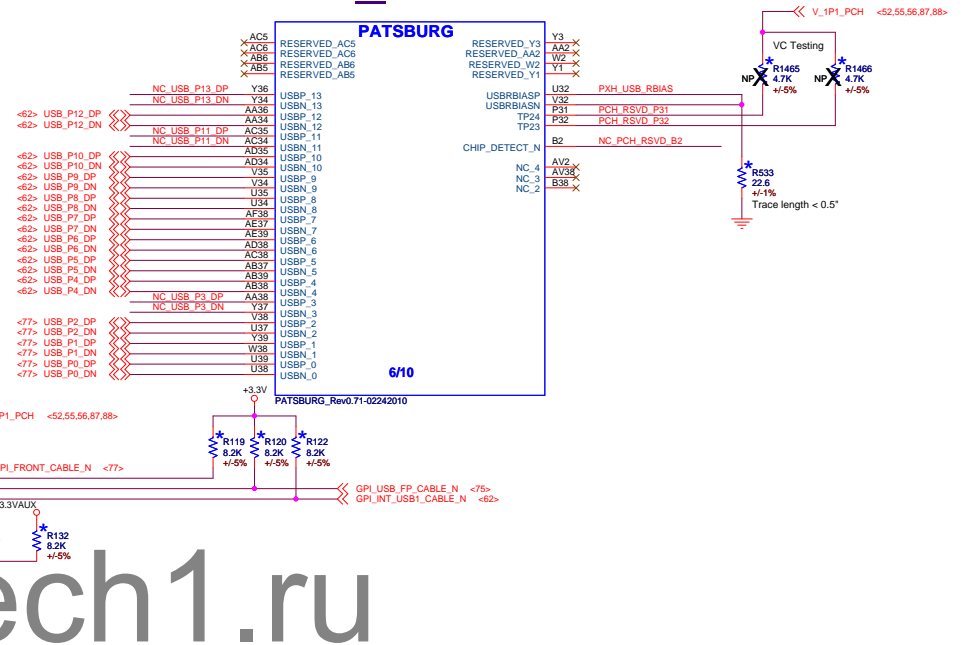


todo: Srini: Check SAS NB\SB

SAS Ports 0&1 @ 6GB/s  
SAS Ports 2-5 @ 3GB/s

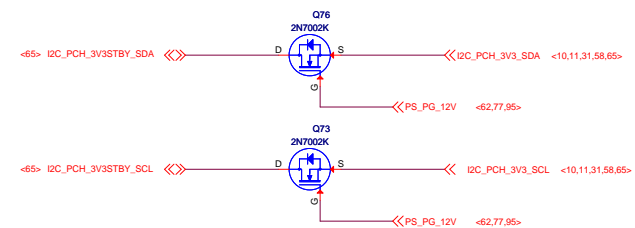


# U\_PCH



todo: Eric: Do we need separate WAKE pins from CPU and PCH lanes?

todo: Eric: Do we need separate WAKE pins for the LOM

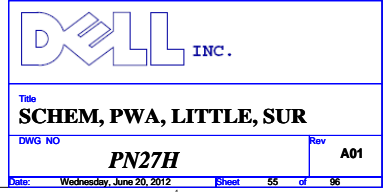


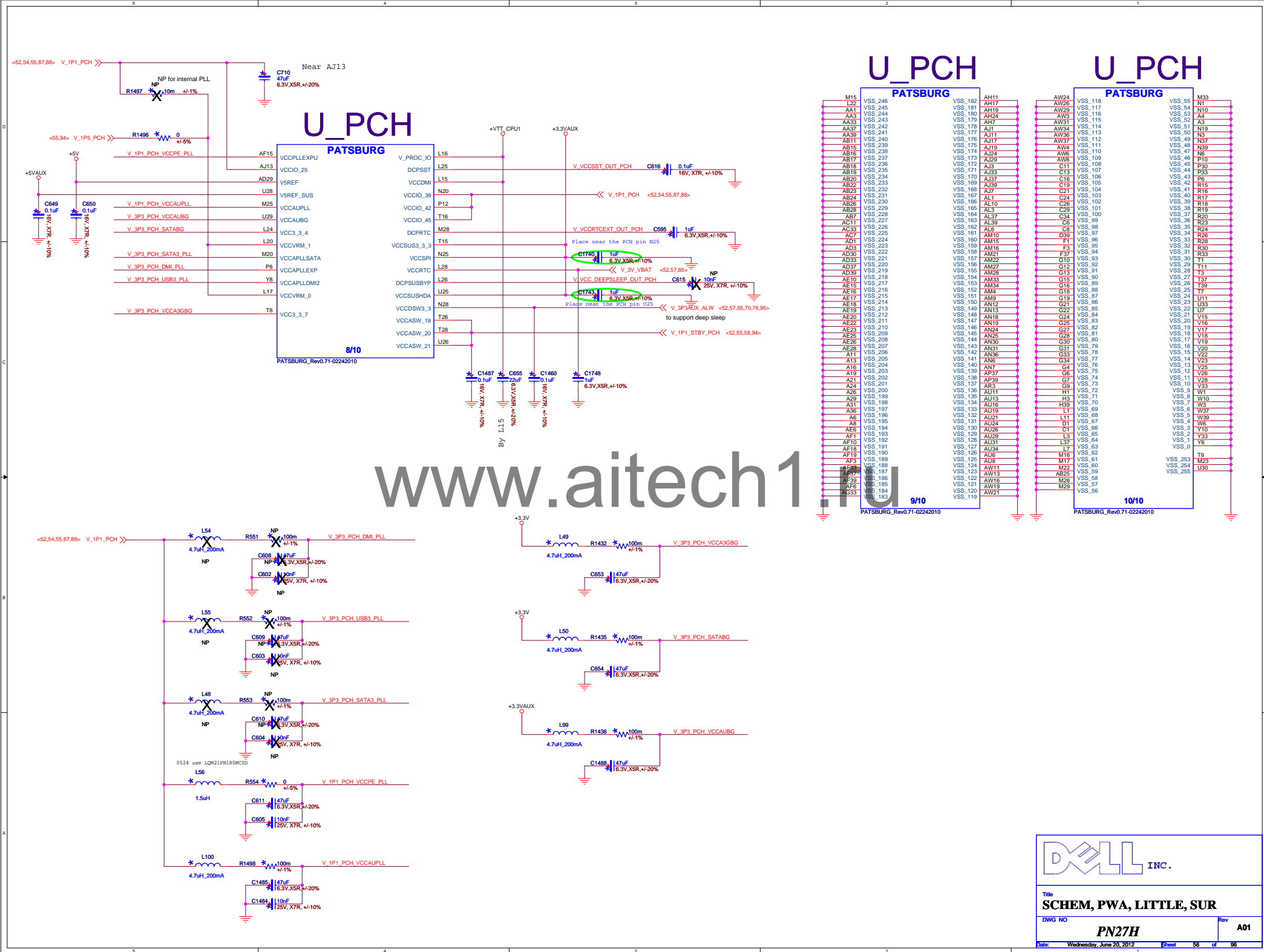
Title  
**SCHEM, PWA, LITTLE, SUR**

**PN27H**

A01

## PATSBURG





# U\_PCH U\_PCH

## U\_PCH

PATSBURG

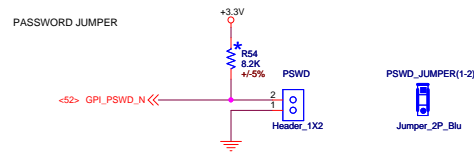
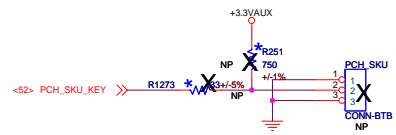
PATSBURG

8/10

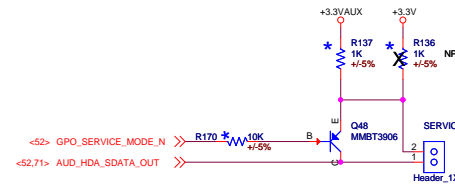
9/10

10/10

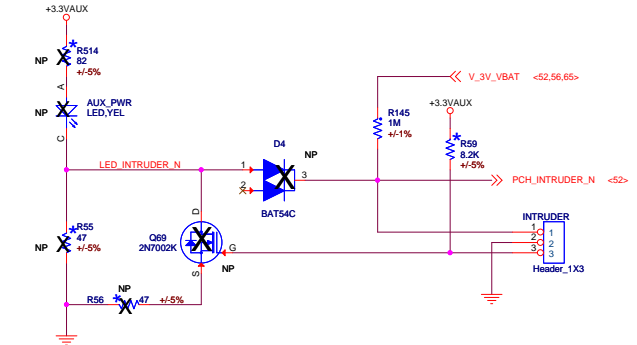




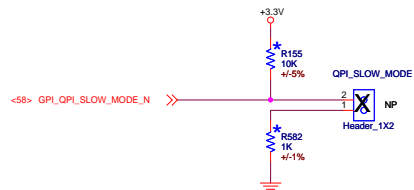
SERVICE MODE JUMPER  
ME FIRMWARE UPDATE on CRB



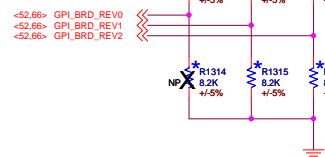
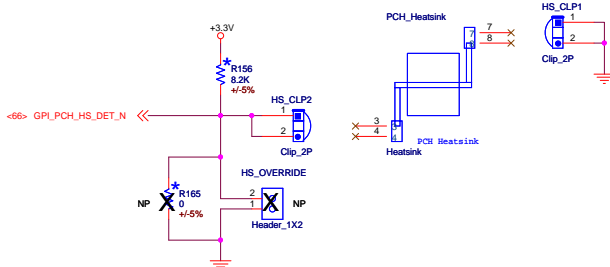
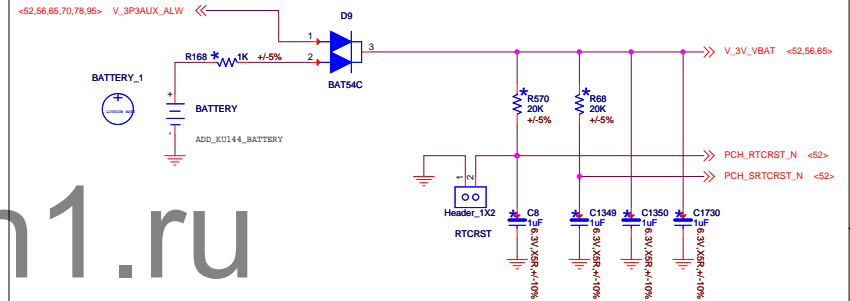
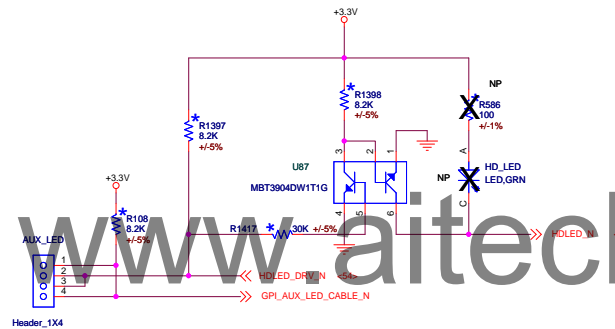
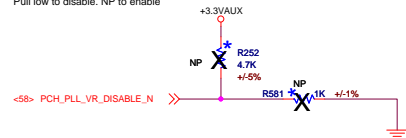
INTRUDER DETECTION SWITCH and AUX LED



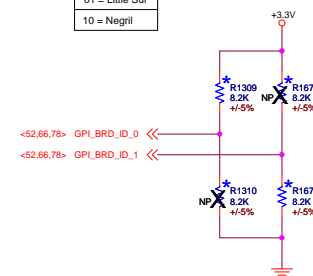
GPI SLOW MODE SELECT



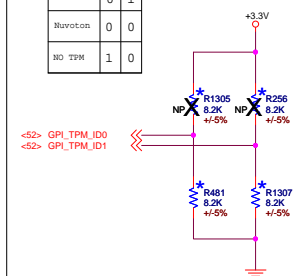
PCH On-Die PLL VR  
Pull low to disable. NP to enable



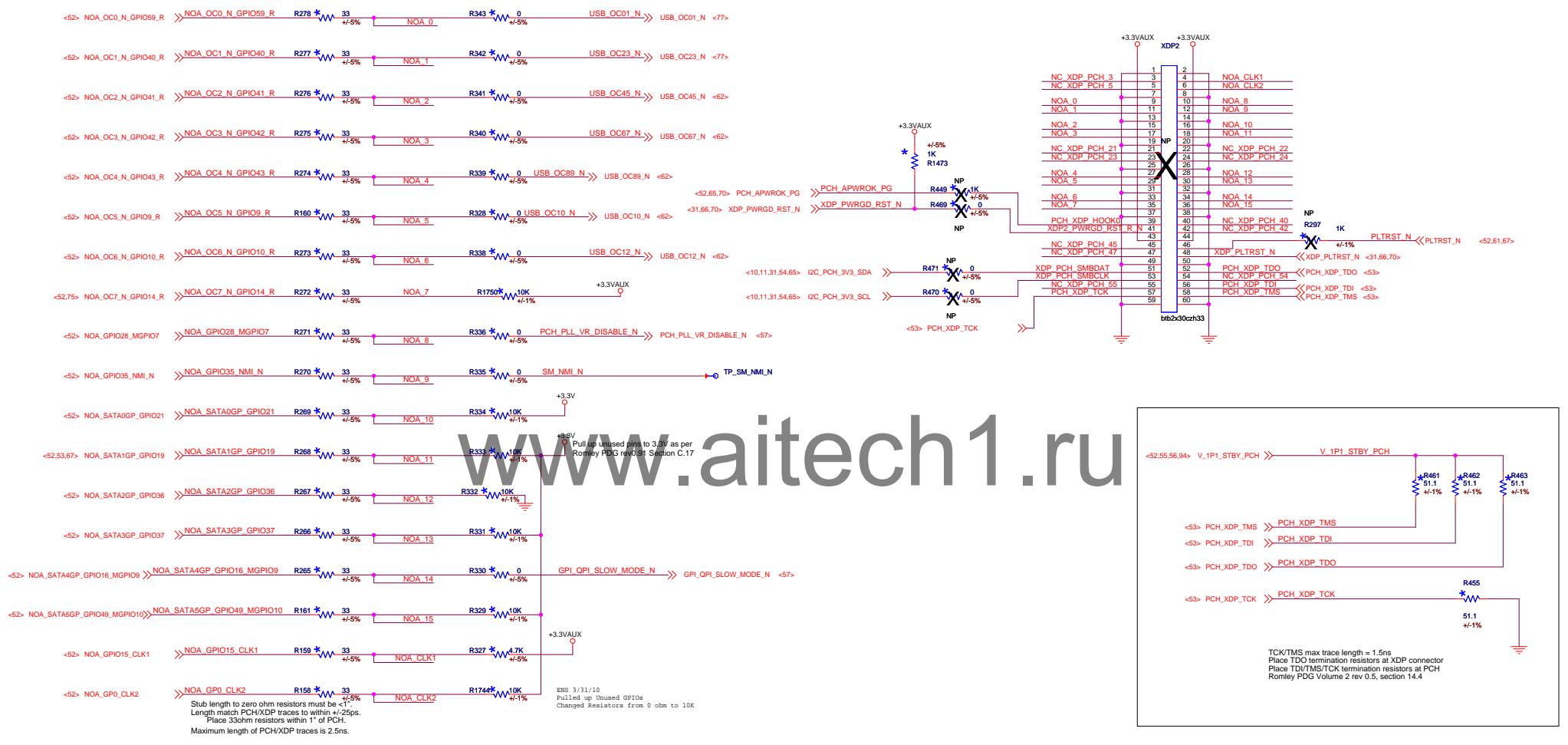
00 = Big Sur  
01 = Little Sur  
10 = Negril



Vendor	ID
00	1
01	0
10	0

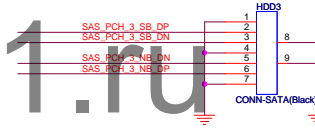
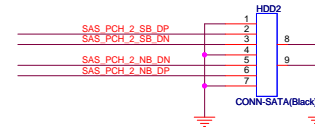
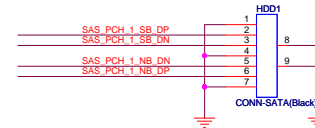
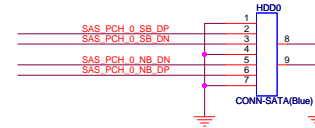
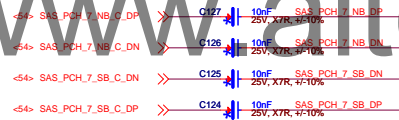
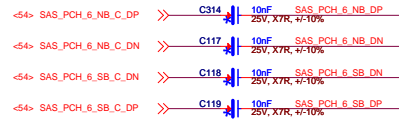
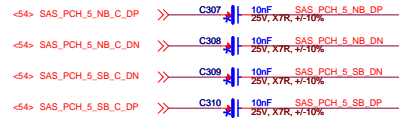
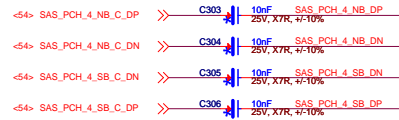
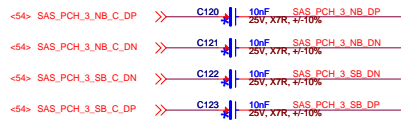
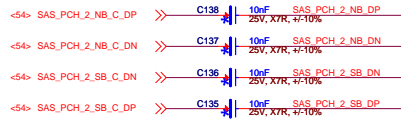
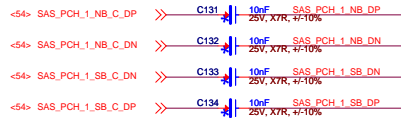
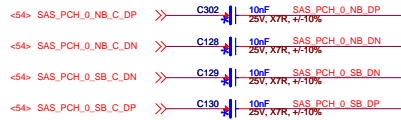


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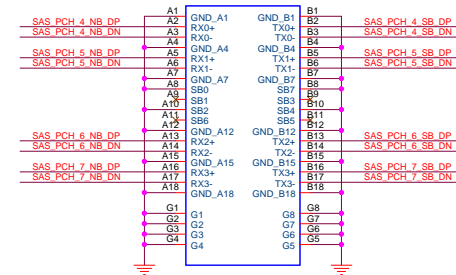


Place series Res by PCH. (See PDG)





## SAS1



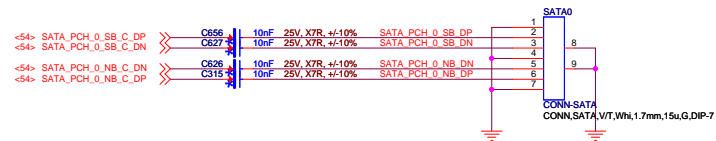
Title  
**SCHEM, PWA, LITTLE, SUR**

DWG NO

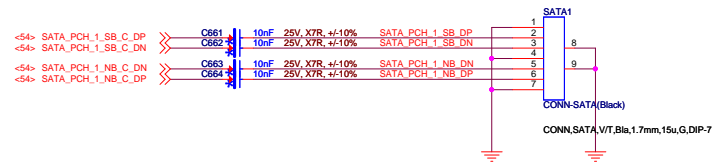
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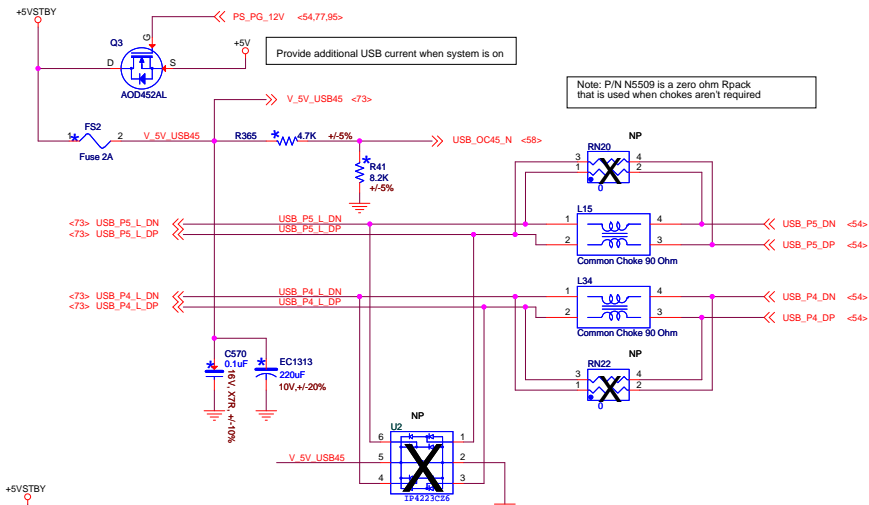


SATA 6G connector  
LE18077-A50D-4F  
LE18077-W50D-4F  
LE18077-Z50D-4F

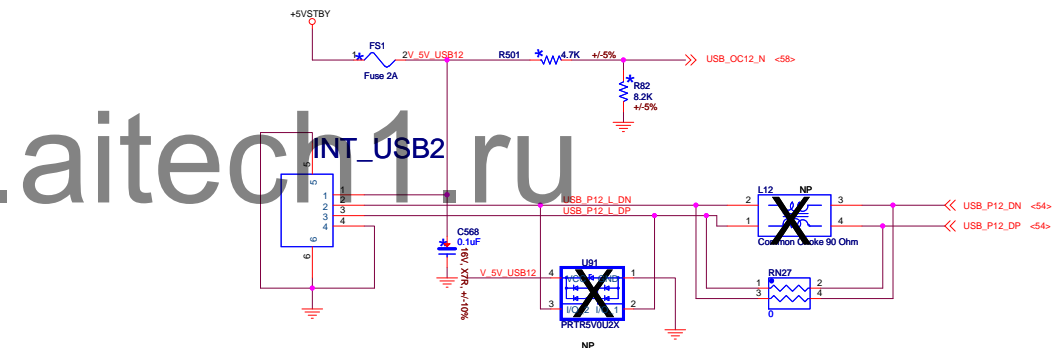
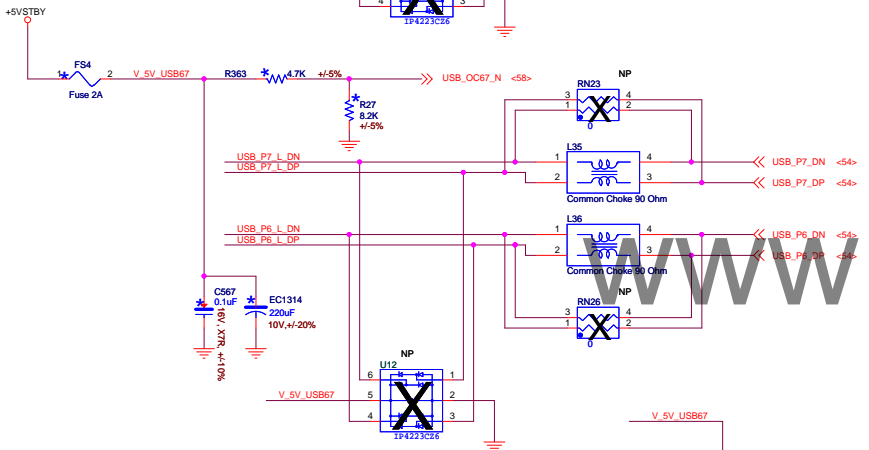
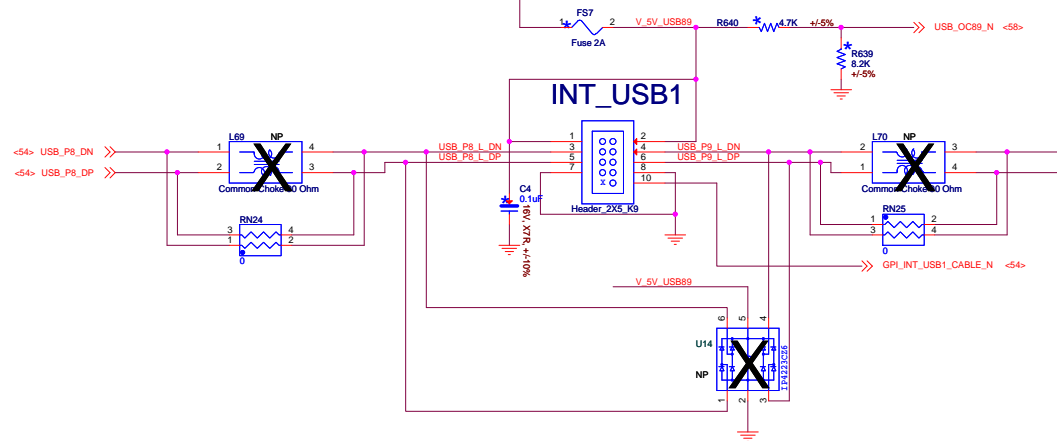


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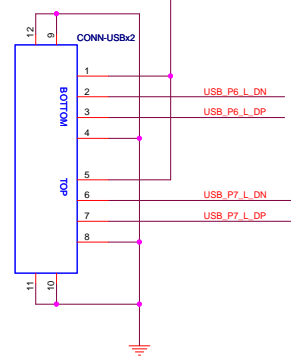




Note: P/N N5509 is a zero ohm Rpack that is used when chokes aren't required



## REAR\_USB1



### USB PORTS TABLE

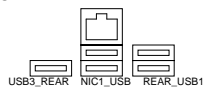
Port	Location
0 - 3	Front USB (pg77)
4 - 5	Rear NIC1_USB x2
6 - 7	Rear NIC2_USB x2 (BigSur)
8 - 9	INT_USB1 x2 (LittleSur)
10	USB3_REAR
12	INT_USB2 (Internal USB)

Ports 1 and 9 are USB debug ports

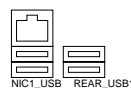
### BIGSUR REAR USB PORTS



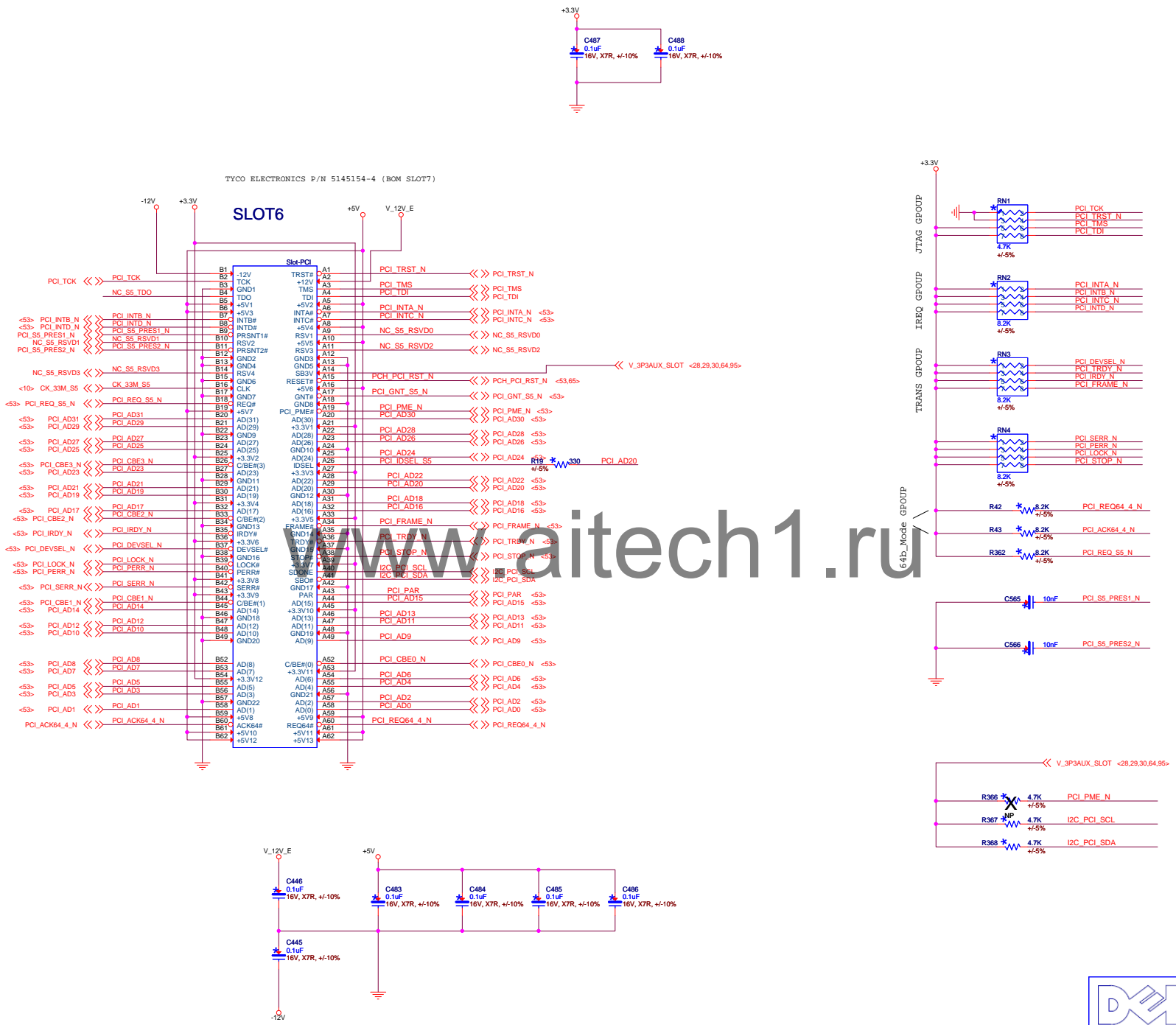
### LITTLESUR REAR USB PORTS




### NEGRIL REAR USB PORTS



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**PN27H**  
 Date: Wednesday, June 20, 2012 Sheet 62 of 96



PCI32 SLOT



INC.

Title

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DWG NO

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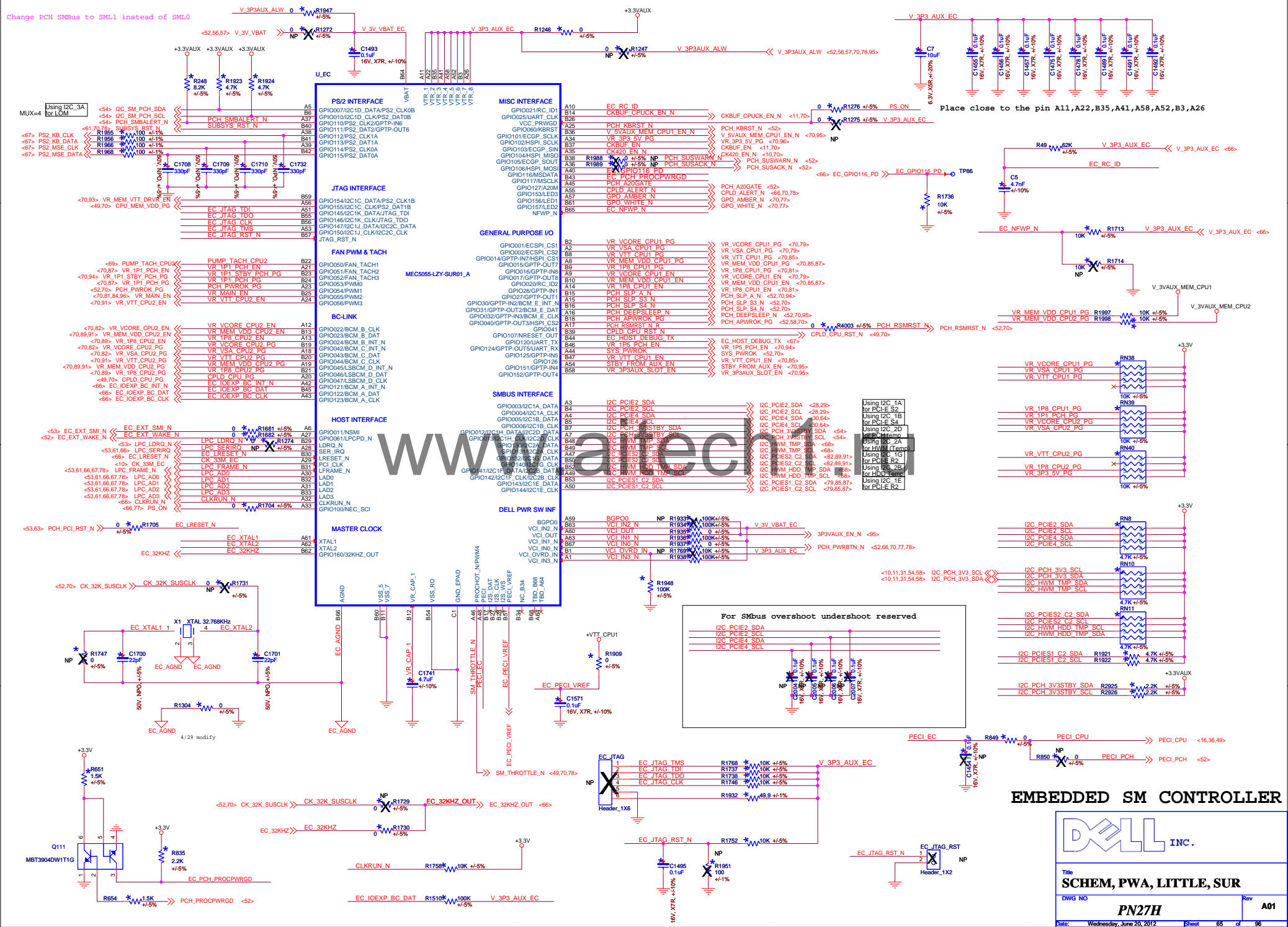
Rev

**A01**

Date: Wednesday, June 20, 2012

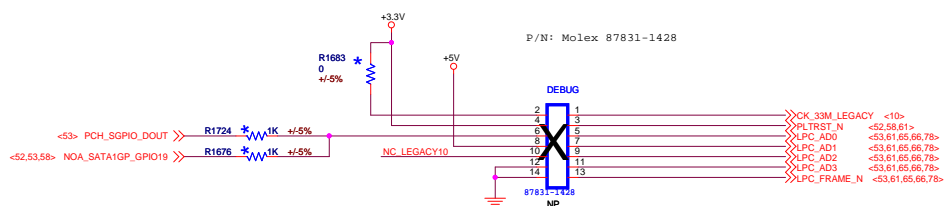
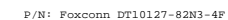
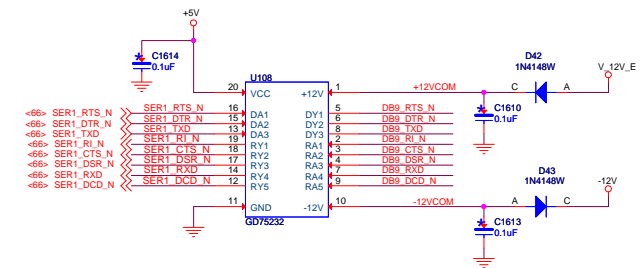
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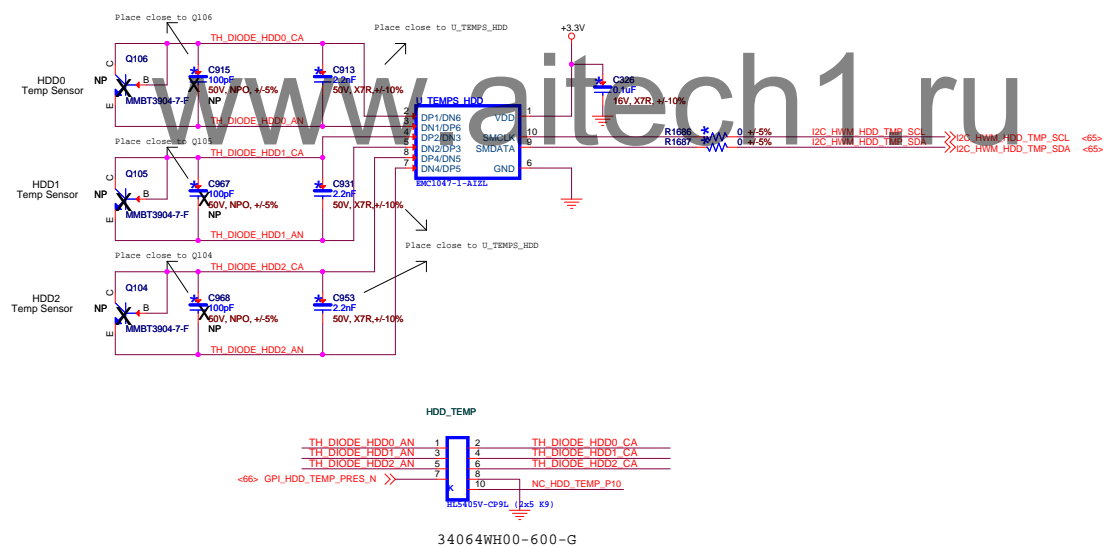




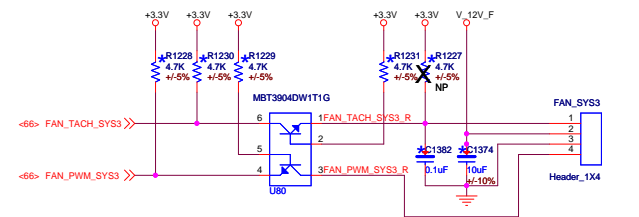
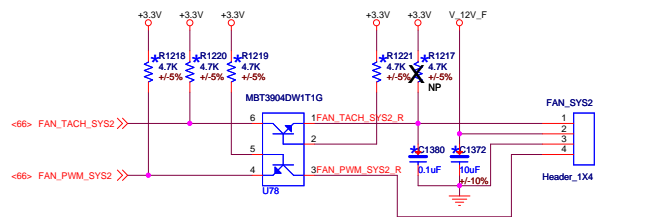
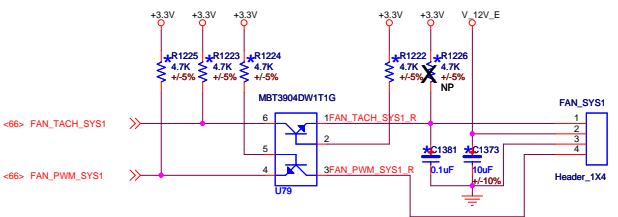
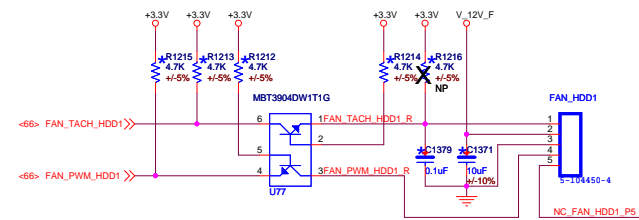
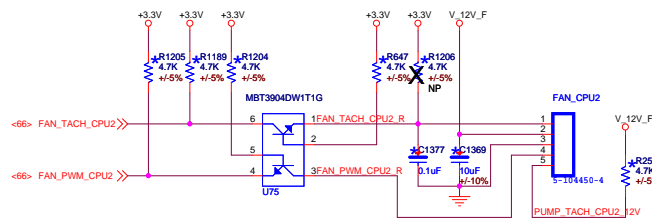
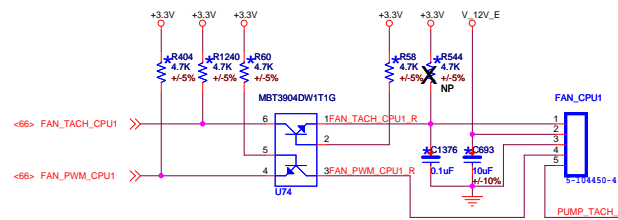




A01



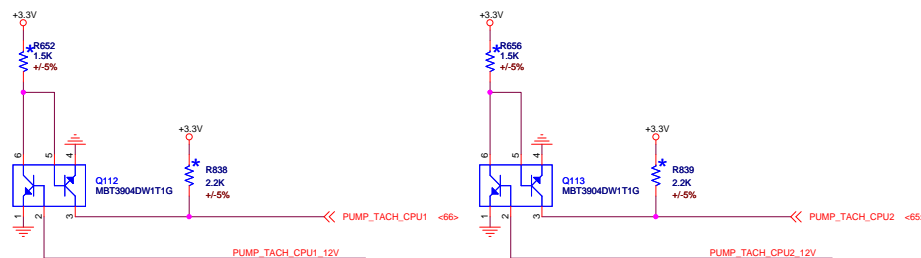
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Fan Matrix

Little Sur	5048 PWM/TACH 3	5048 PWM/TACH 1	5048 PWM/TACH 2	5048 PWM/TACH 3	5048 PWM/TACH 4	5048 PWM/TACH 6
	CPU1 Fan	CPU2 Fan	SYS1 FAN	SYS2 FAN	SYS3 FAN	HDD1 FAN

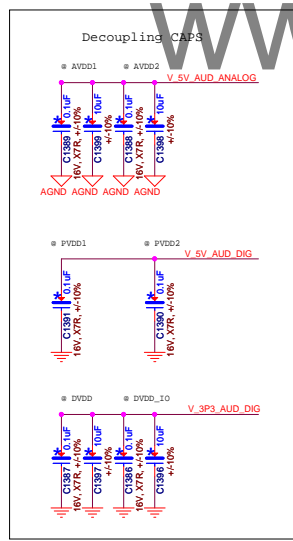
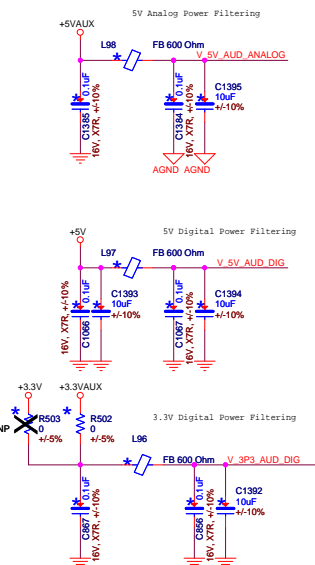
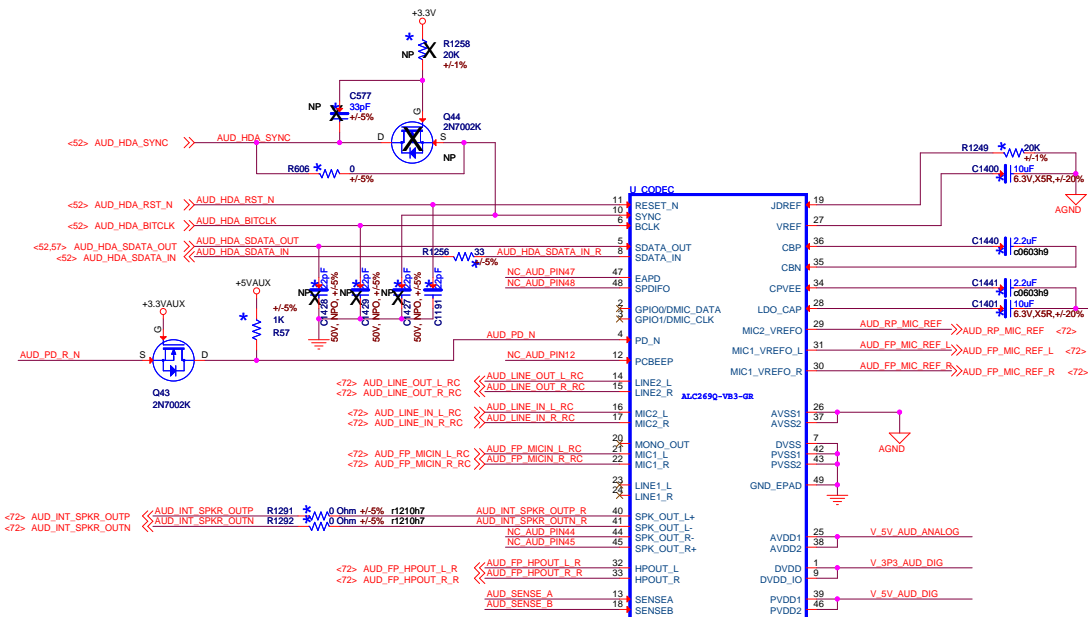


## FAN CONNECTOR

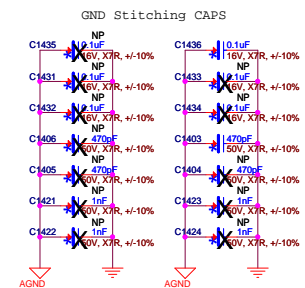
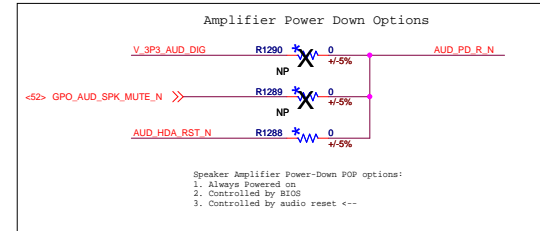
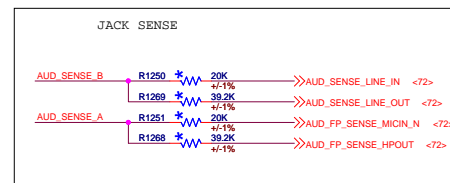
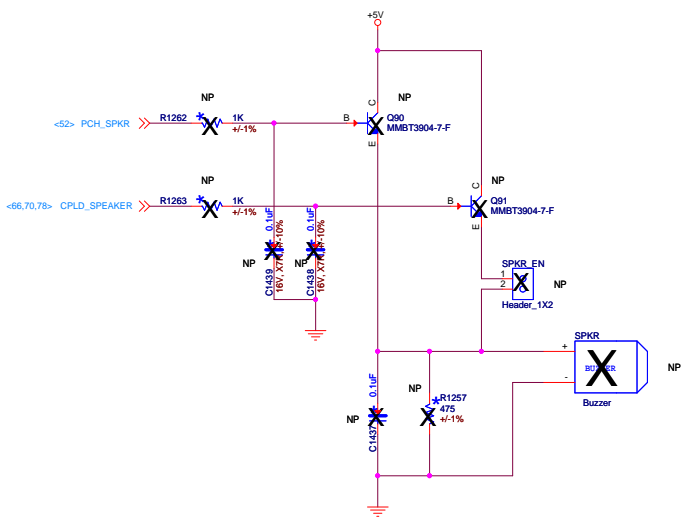


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**AUDIO CODEC**

**DELL INC.**

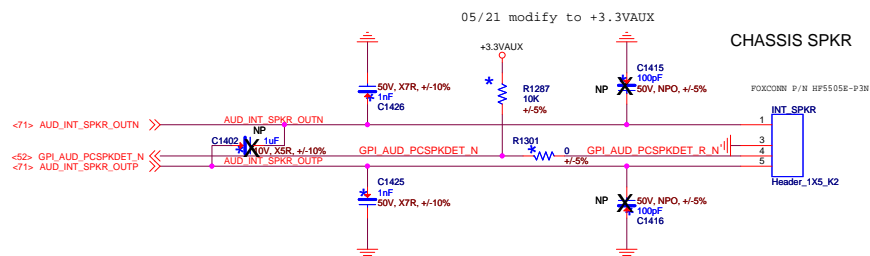
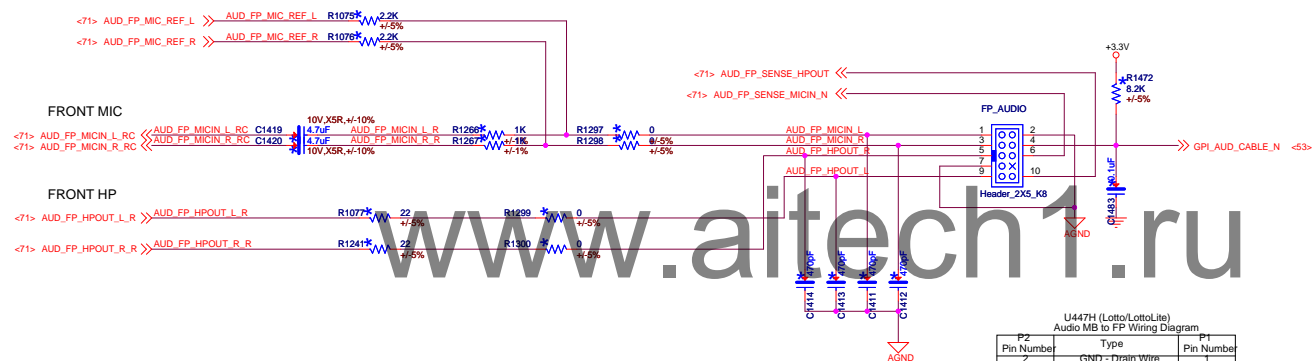
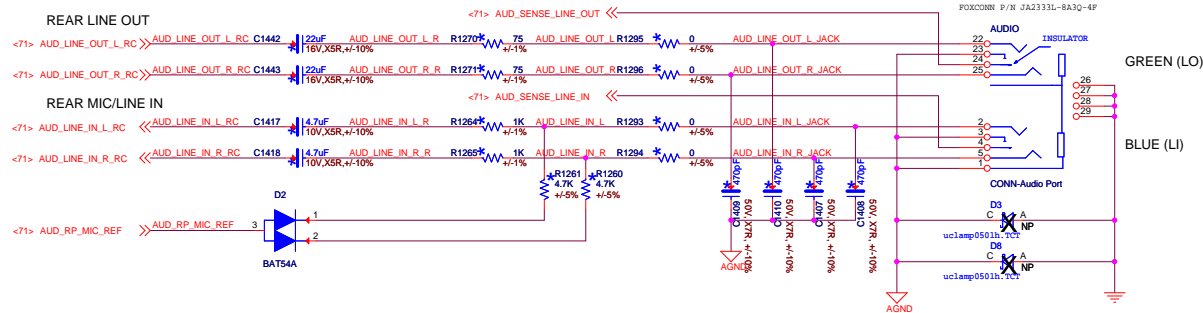
Title: **SCHEM, PWA, LITTLE, SUR**

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## AUDIO FILTER AND CONNS



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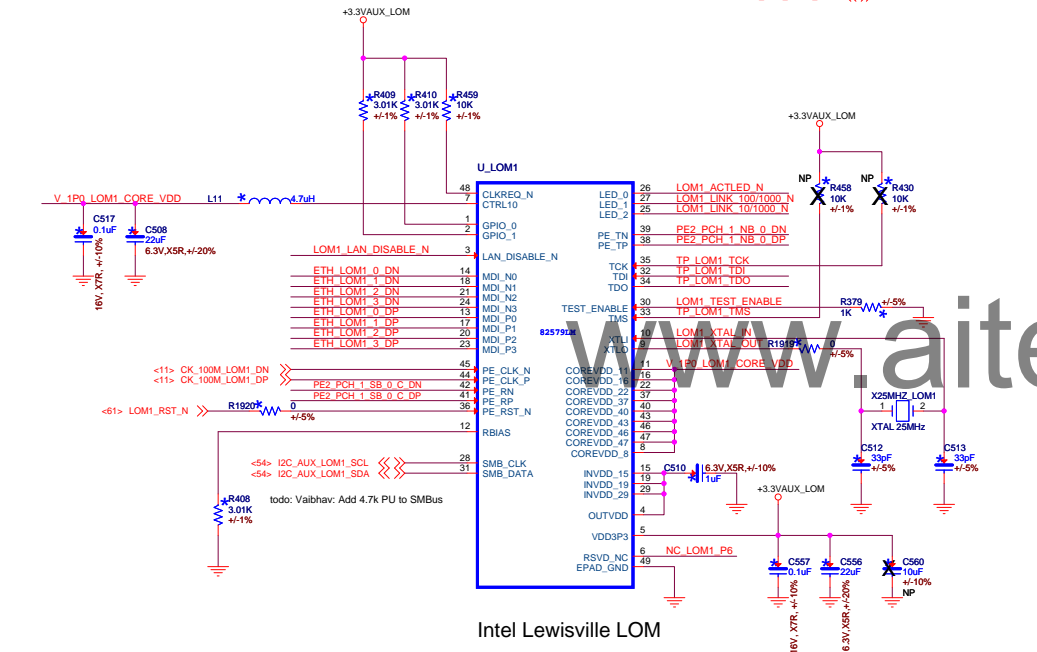
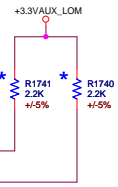
LOM1\_ACTLED\_N R397 330 LOM1\_ACTLED\_R\_N  
 <77> LOM1\_LINK\_10/1000\_N <<LOM1\_LINK\_10/1000\_NR398 330 LOM1\_LED\_GRN\_N  
 <77> LOM1\_LINK\_100/1000\_N <<LOM1\_LINK\_100/1000\_R399 330 LOM1\_LED\_ORG\_N

LOM1 LED Current limiting resistors  
 adjust resistors for LED brightness

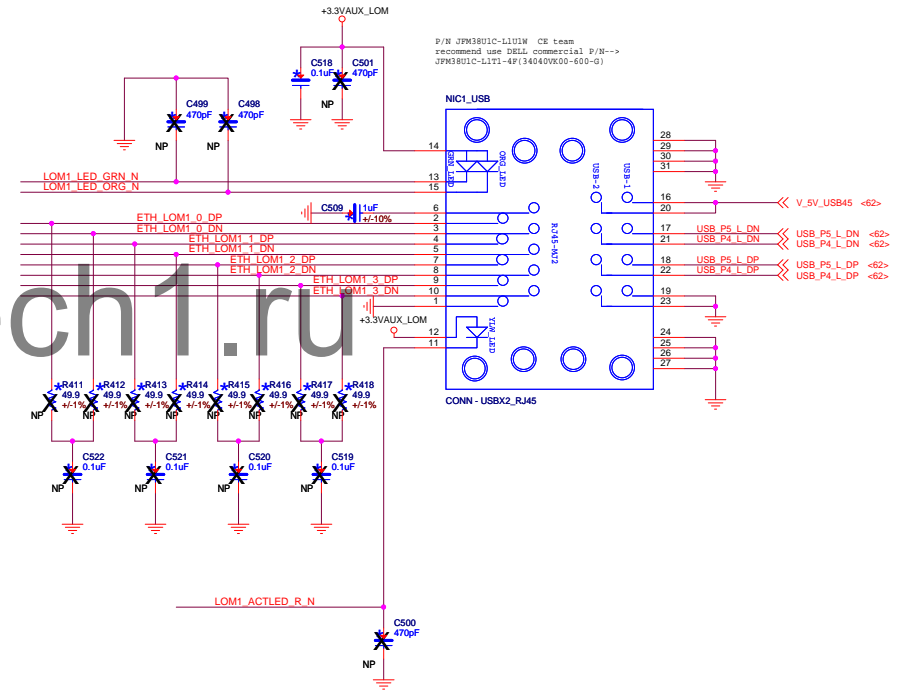
<53> PE2\_PCH\_1\_NB\_0\_C\_DP << C523 0.1uF PE2\_PCH\_1\_NB\_0\_DP  
 <53> PE2\_PCH\_1\_NB\_0\_C\_DN << C524 0.1uF PE2\_PCH\_1\_NB\_0\_DN  
 <53> PE2\_PCH\_1\_SB\_0\_C\_DP << C526 0.1uF PE2\_PCH\_1\_SB\_0\_C\_DP  
 <53> PE2\_PCH\_1\_SB\_0\_C\_DN << C525 0.1uF PE2\_PCH\_1\_SB\_0\_C\_DN

To LOM1

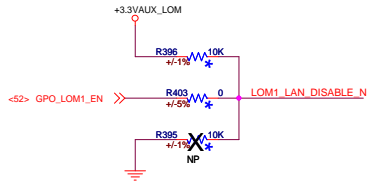
[0412] Add 4.7k PU on nets  
 I2C\_AUX\_LOM1\_SCL/SDA



Intel Lewisville LOM



P/N JPM38U1C-L1U1W CE team  
 recommend use DELL commercial P/N-->  
 JPM38U1C-L1T1-4P(34040VX00-600-0)



LOM1


Title:  
**SCHEM, PWA, LITTLE, SUR**

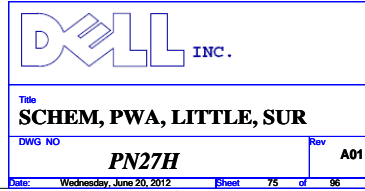
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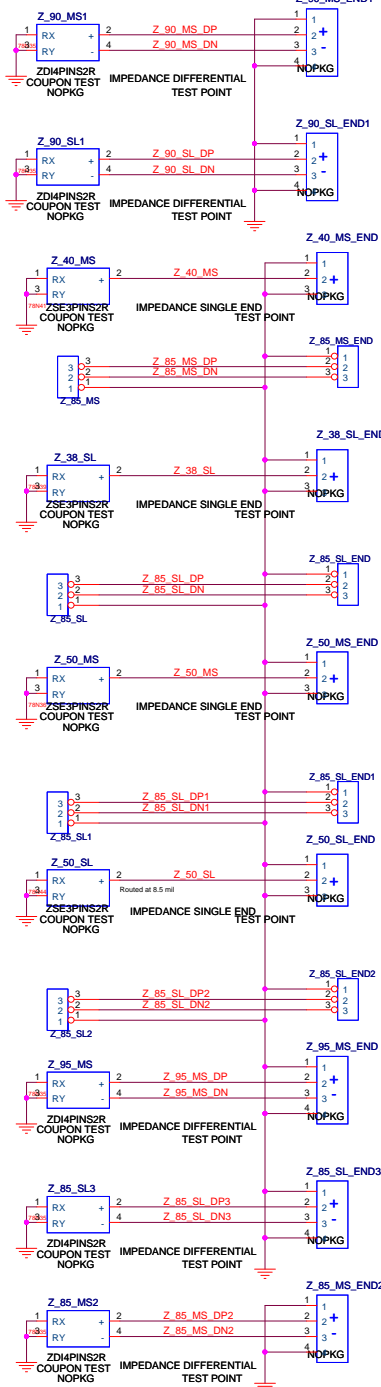
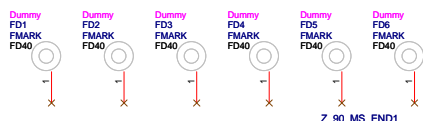
	
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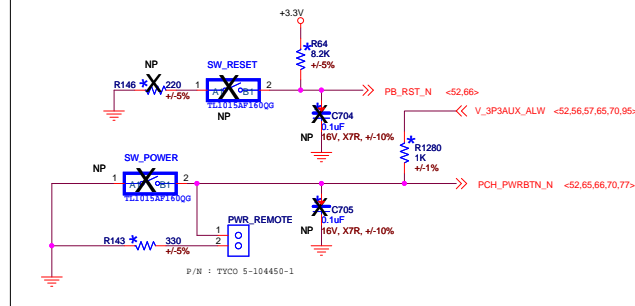
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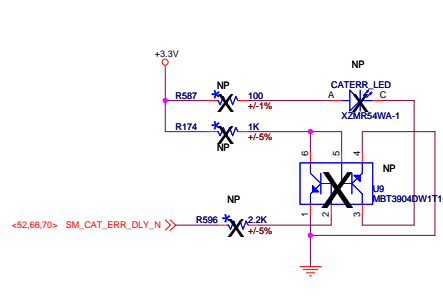




## Debug Switches



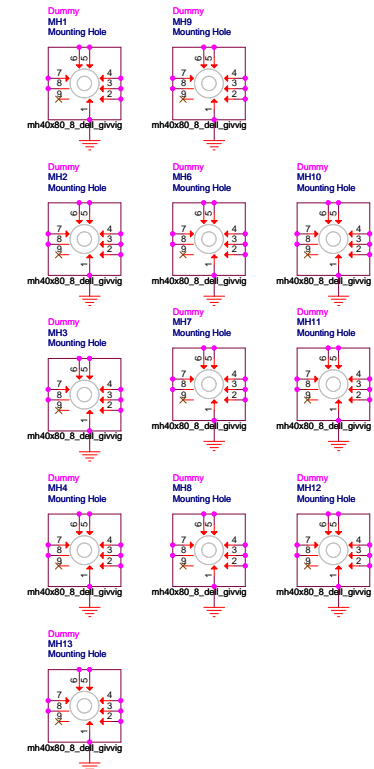
## CATERR LED



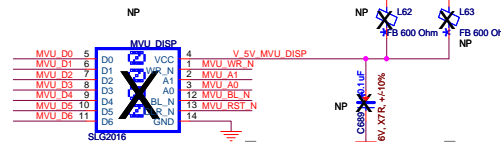
## Part numbers

LittleSur	PWA
	Y56T3 (with TPM)
	V6XGW (no TPM)

## Mounting Holes

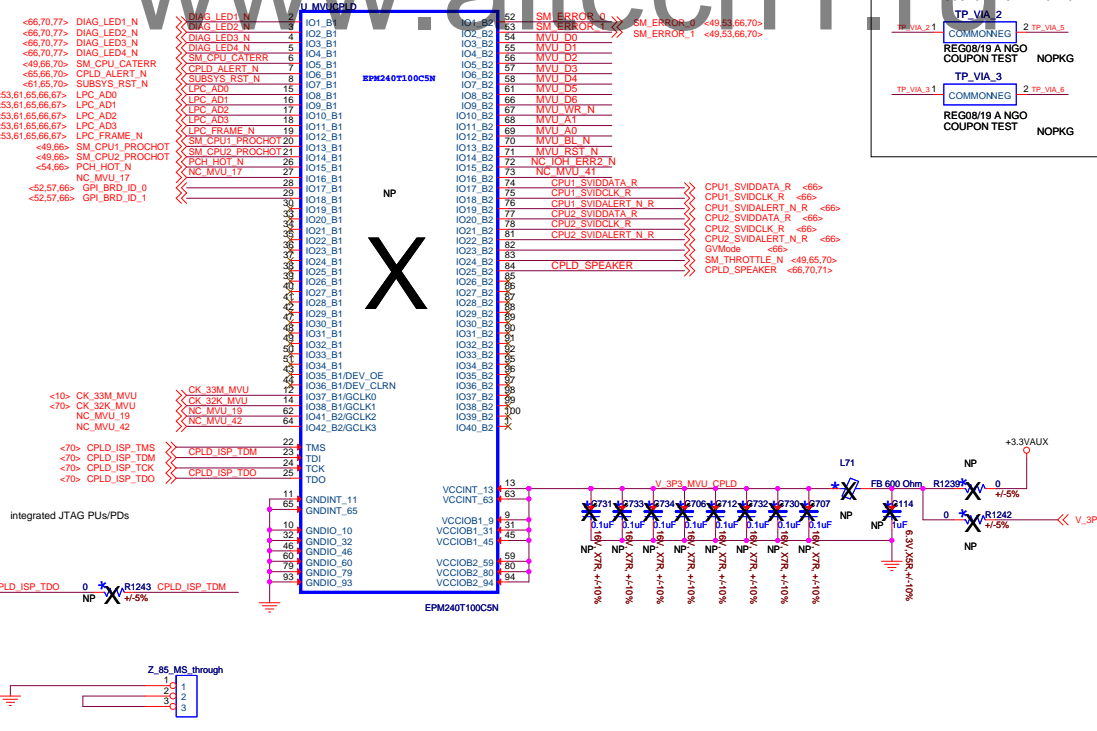
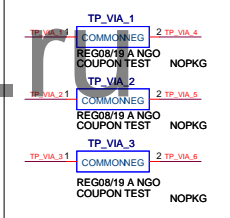


## MicroVu debug display



## PCB registration coupons

Place near BGA's to detect PCB layer registration

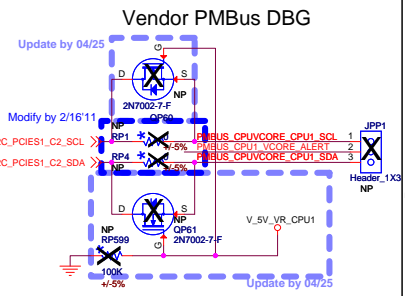
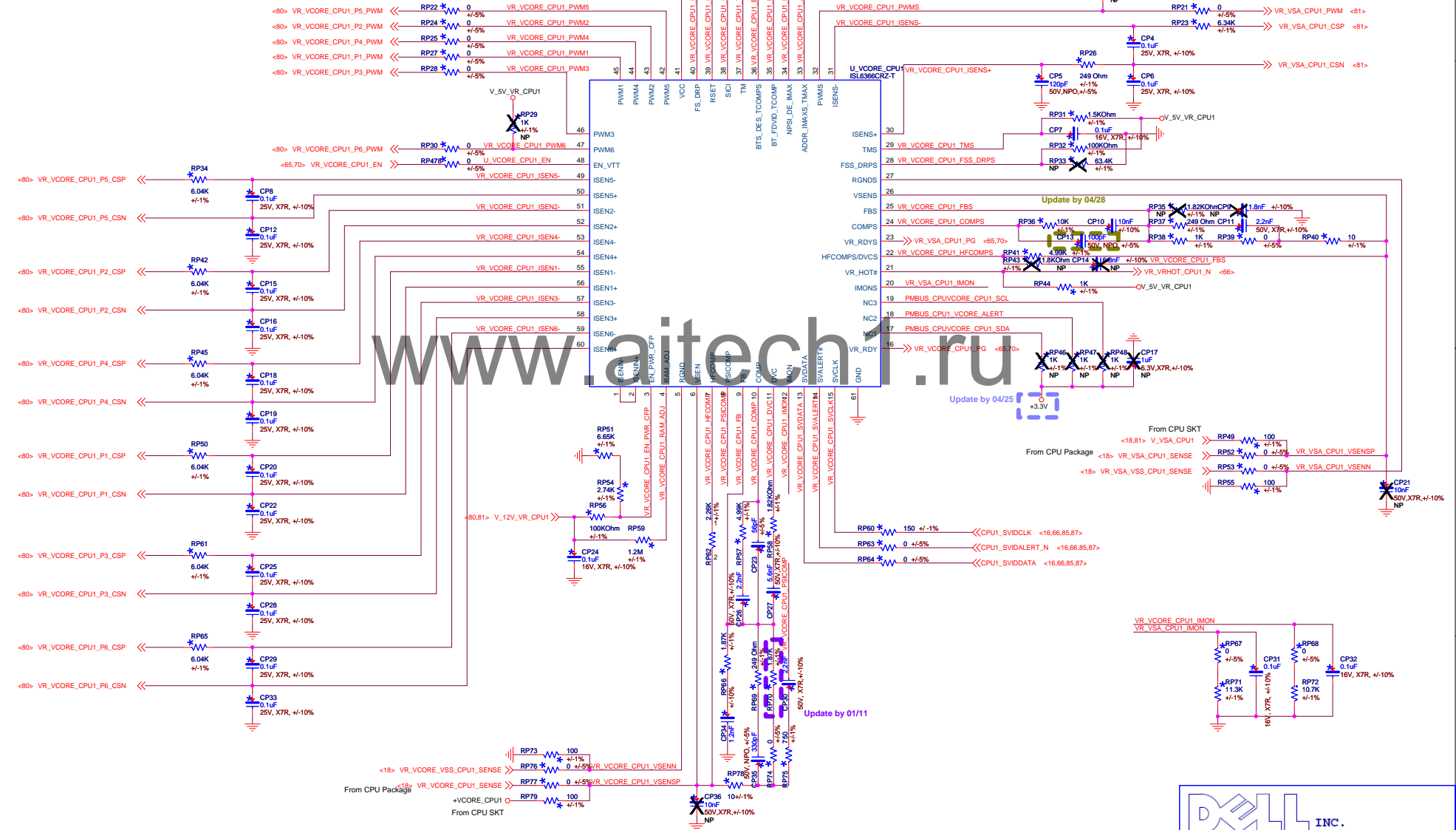


## SPARE, MISC, DEBUG, PROTO



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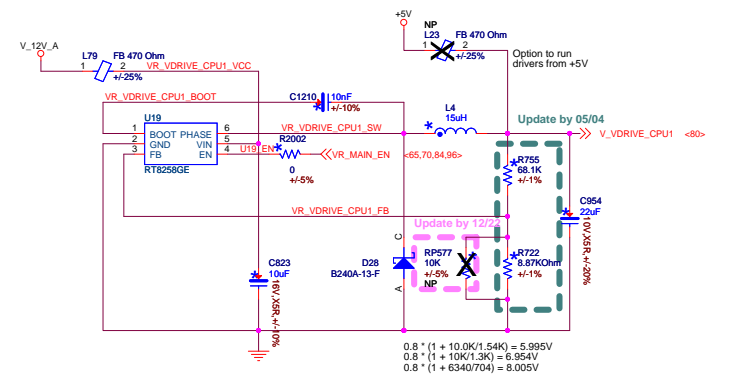
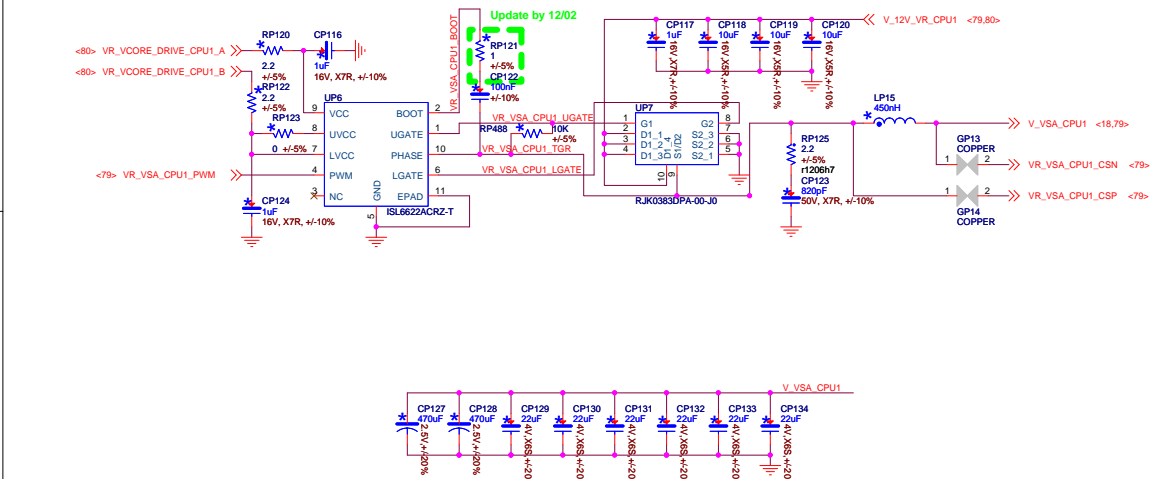
BT=1V, FDVID=20mV/us, Tcomp=29.7C  
NPSI=SI1, DE=enabled, Imax=185A  
ADDR=0/1, Imaxs=25A, SMAddr1=n/a,  
BTS=0.925V, DES=enabled, Tcomps=29.7C



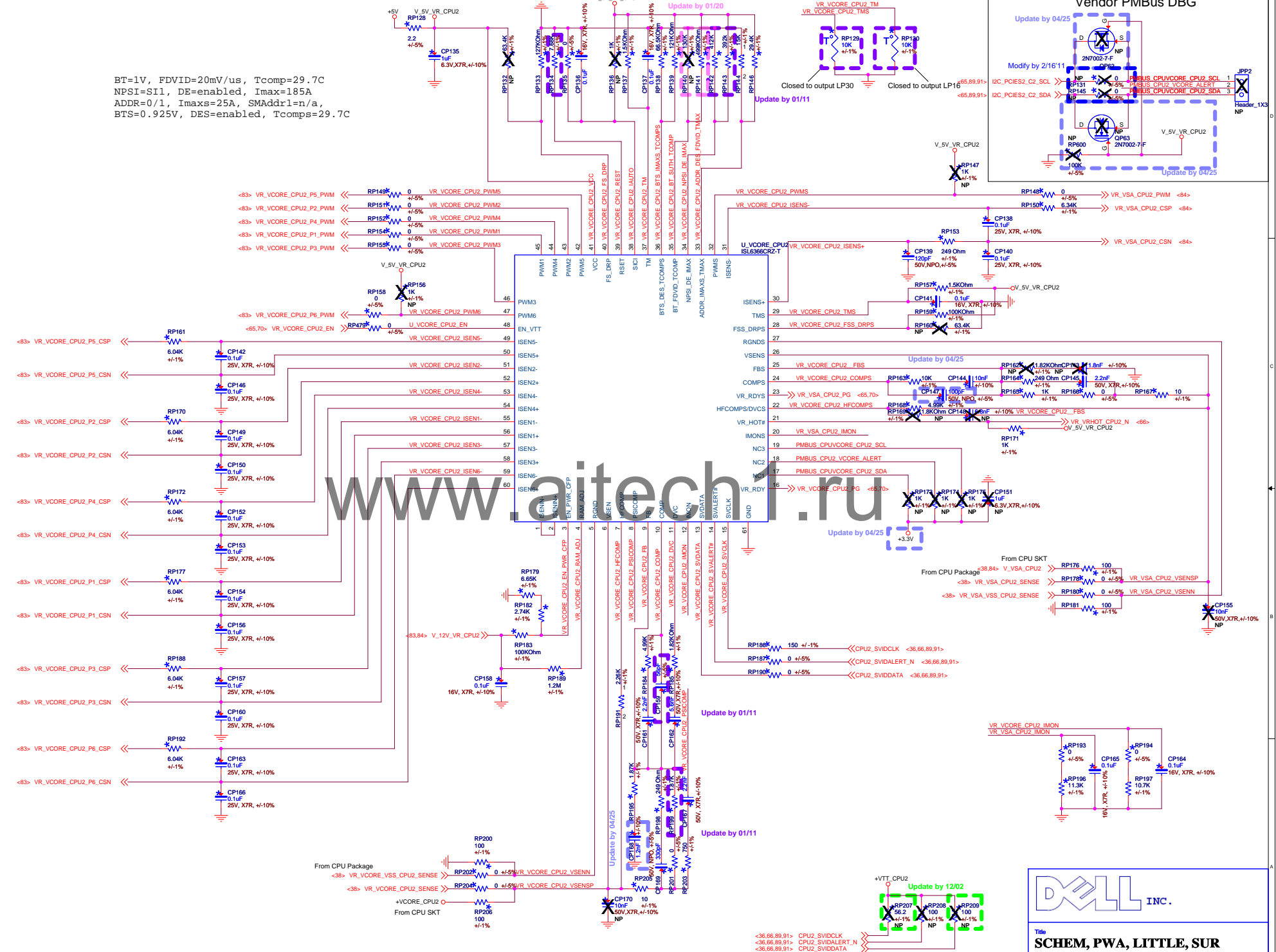




Output	V_VSA_CPU1
Destination	CPU1 VSA rail
Input	12V
Peak Current	VSA 20 A/24 A @ 0.85 V
Thermal Current	tbd
Enabled	



BT=1V, FDVID=20mV/us, Tcomp=29.7C  
NPSI=S11, DE=enabled, Imax=185A  
ADDR=0/1, Imaxs=25A, SMAddr1=n/a,  
BTS=0.925V, DES=enabled, Tcomps=29.7C



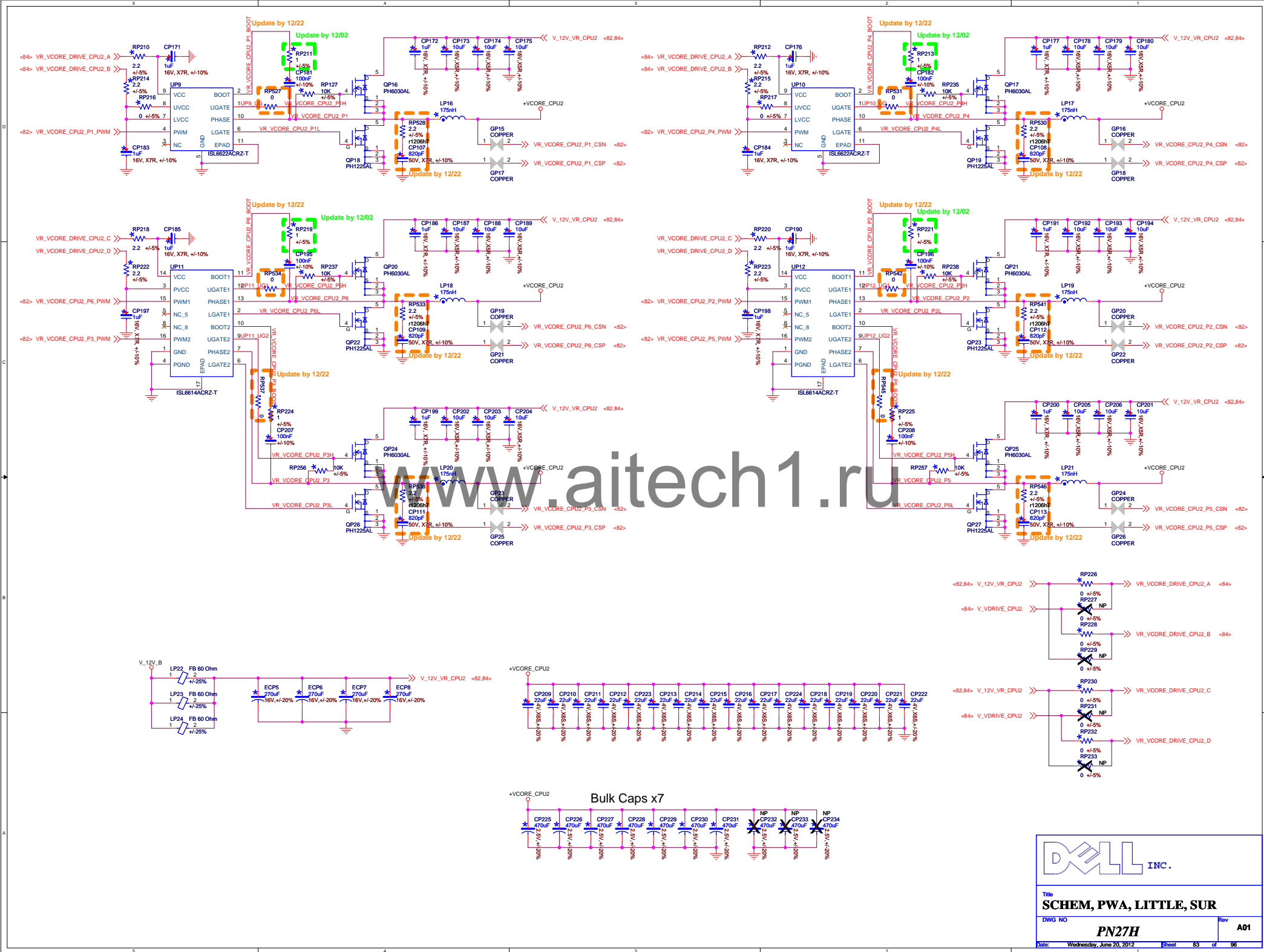
**DELL INC.**

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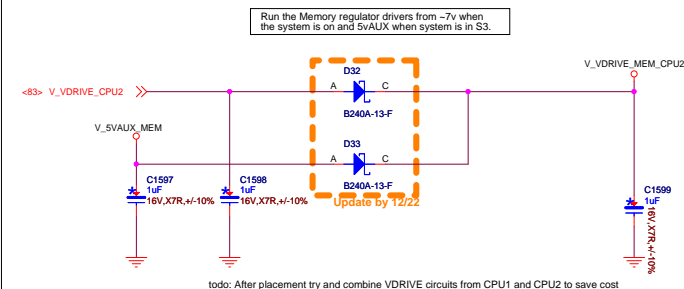
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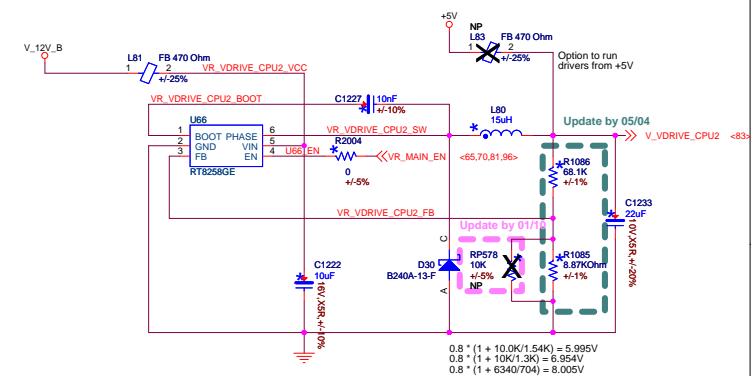


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Output	V_VDRIVE_CPU2
Destination	CPU2 vcore regulator drivers
Input	12V
Peak Current	1.0A
Thermal Current	390mA
Enabled	
Min Current	120mA
Min_OCP	1.6V



todo: After placement try and combine VDRIVE circuits from CPU1 and CPU2 to save costs



**PN27H**

A01

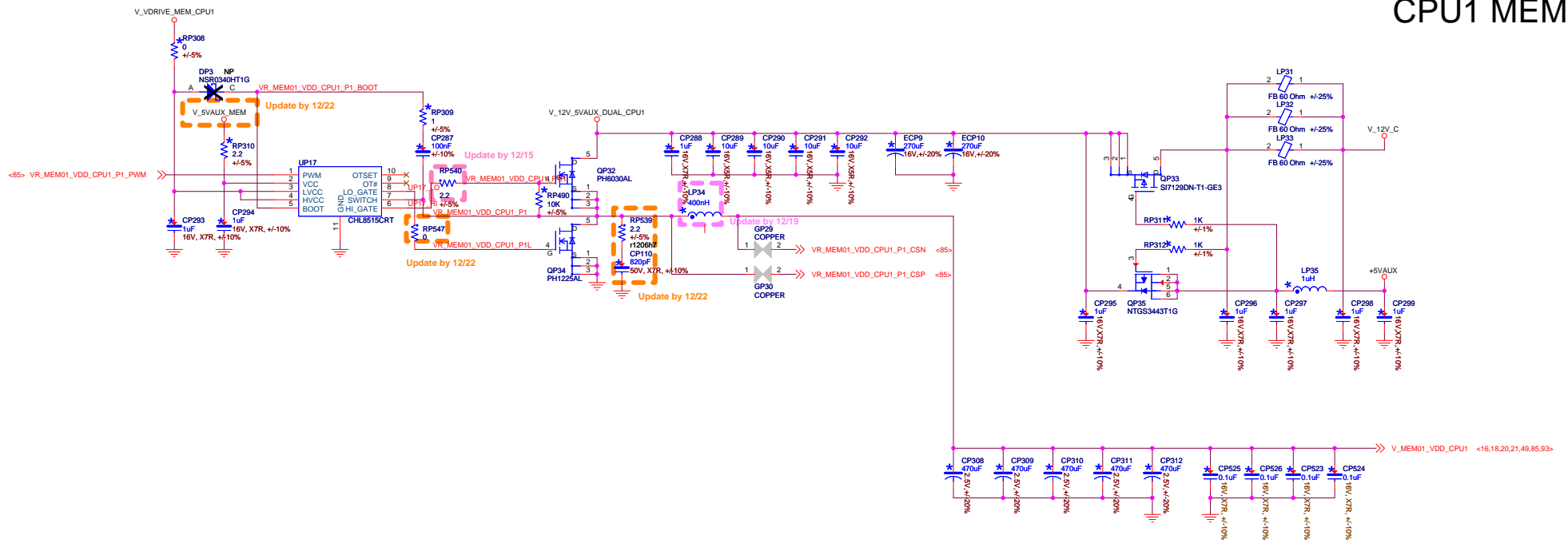
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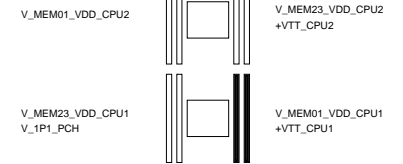
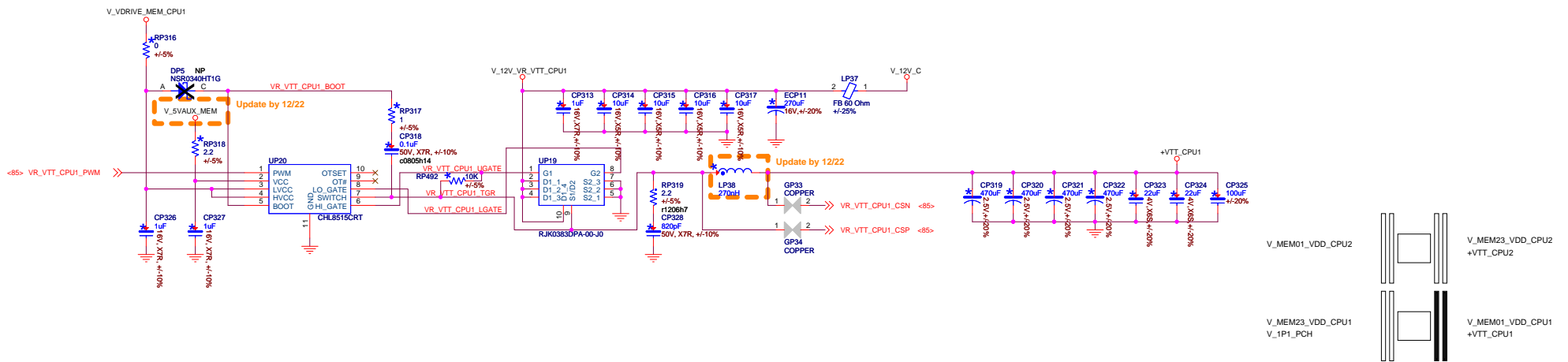
A01

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# CPU1 MEM01

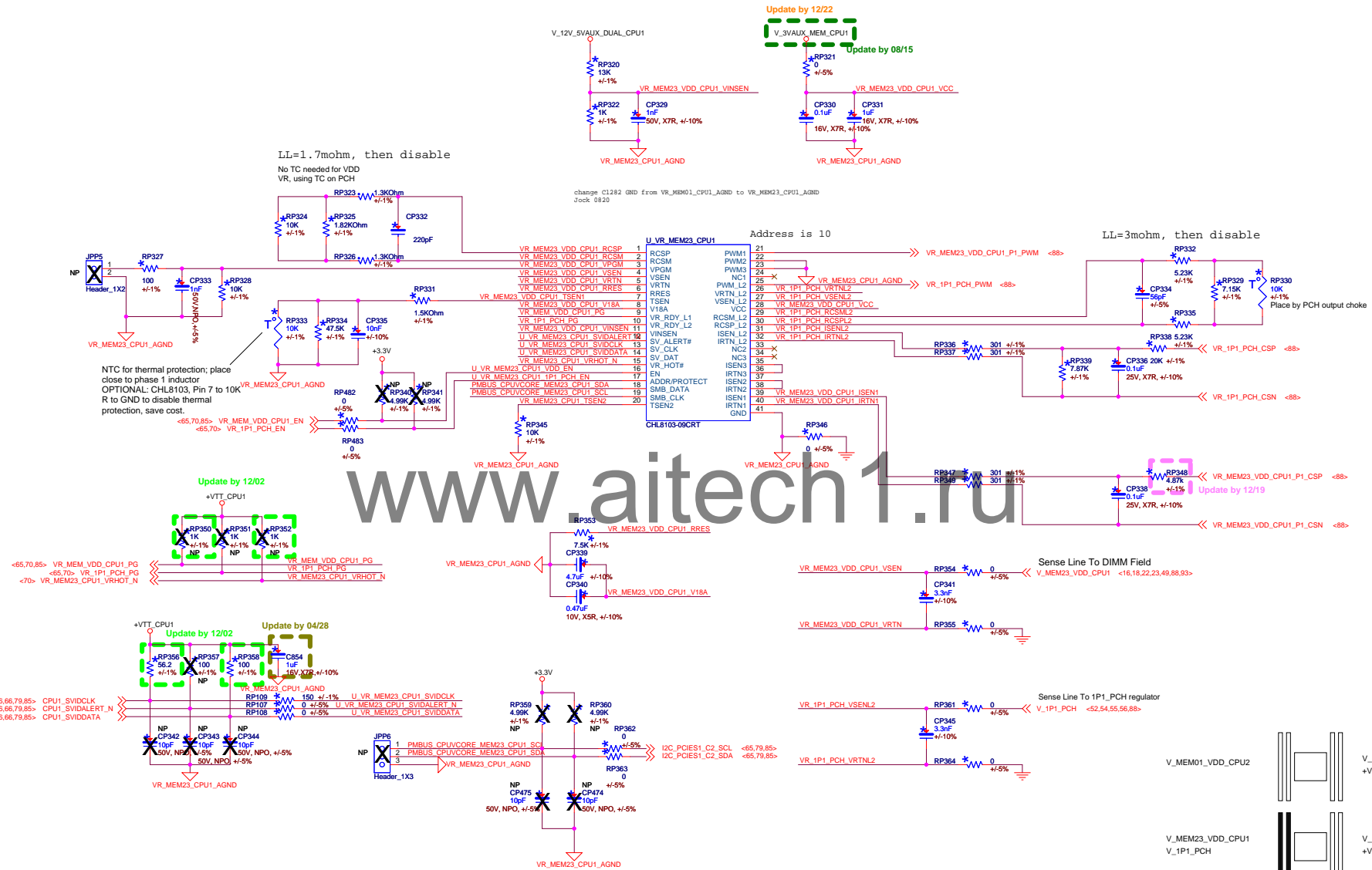


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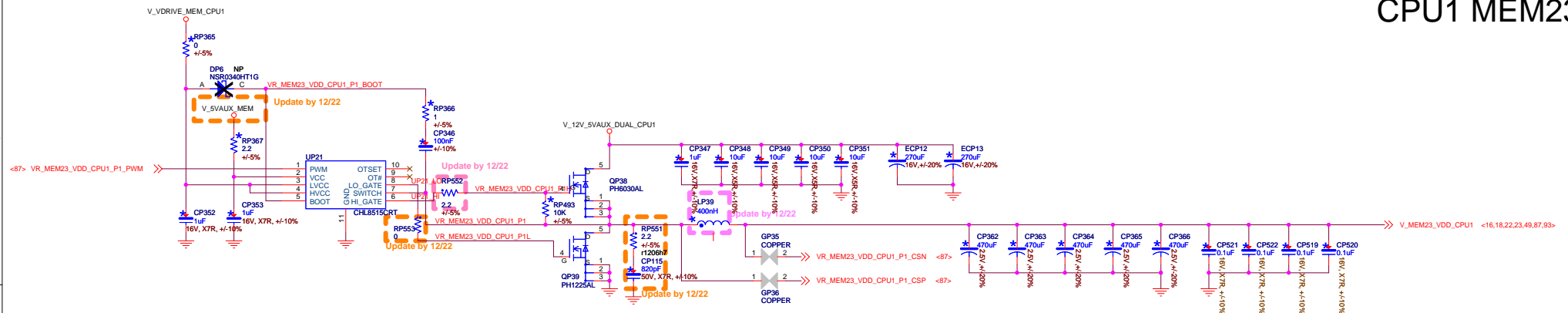


## CPU1 MEM23- CHIL CHL8103

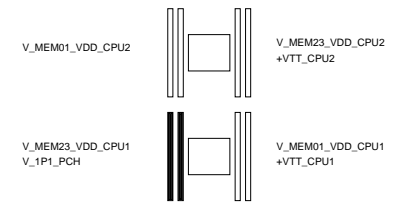
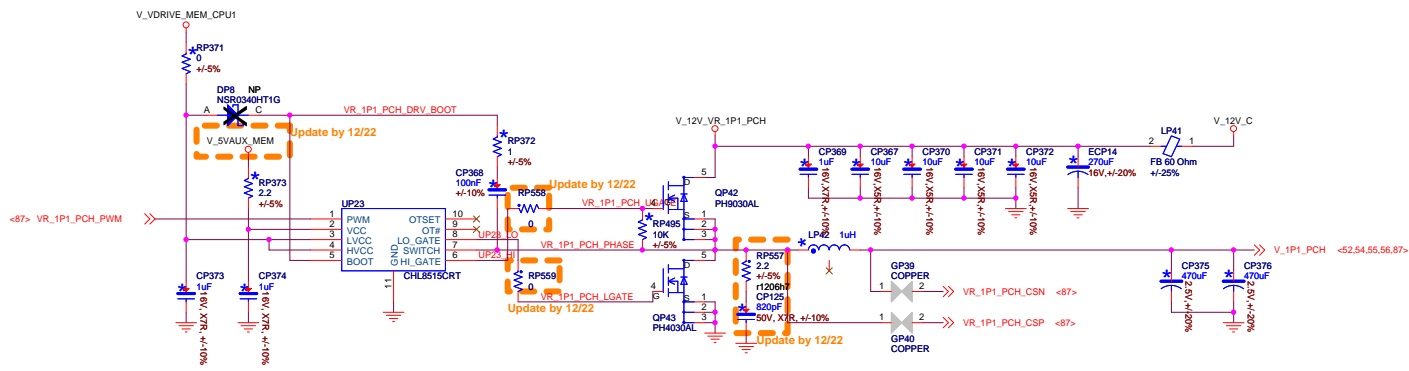


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# CPU1 MEM23



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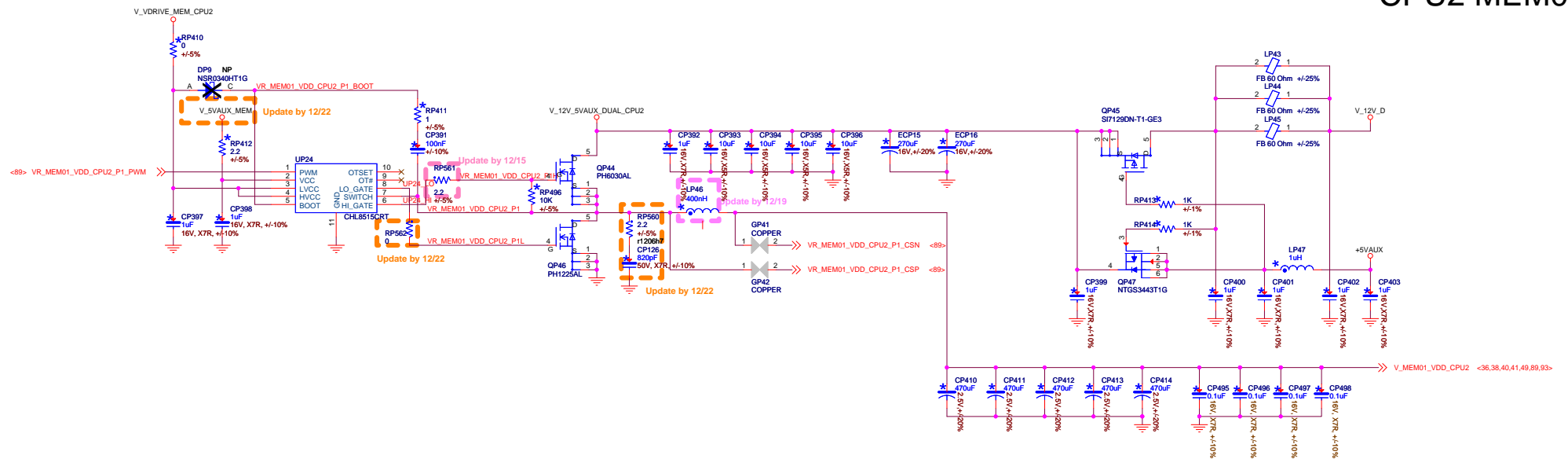


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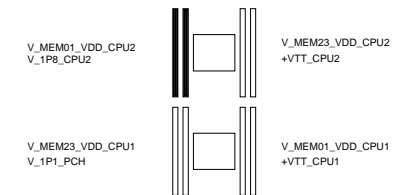
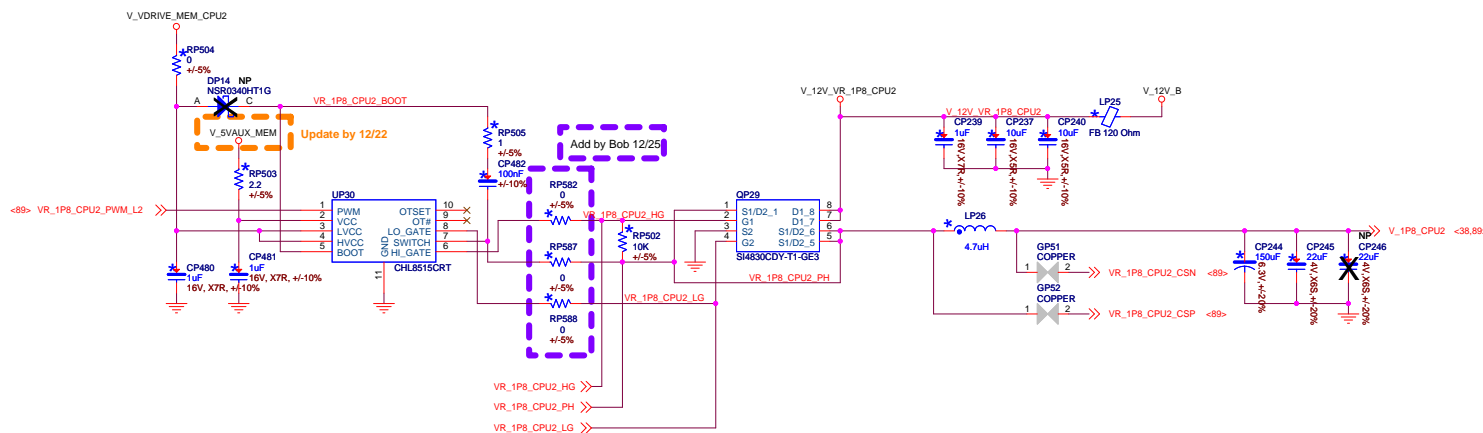


A01

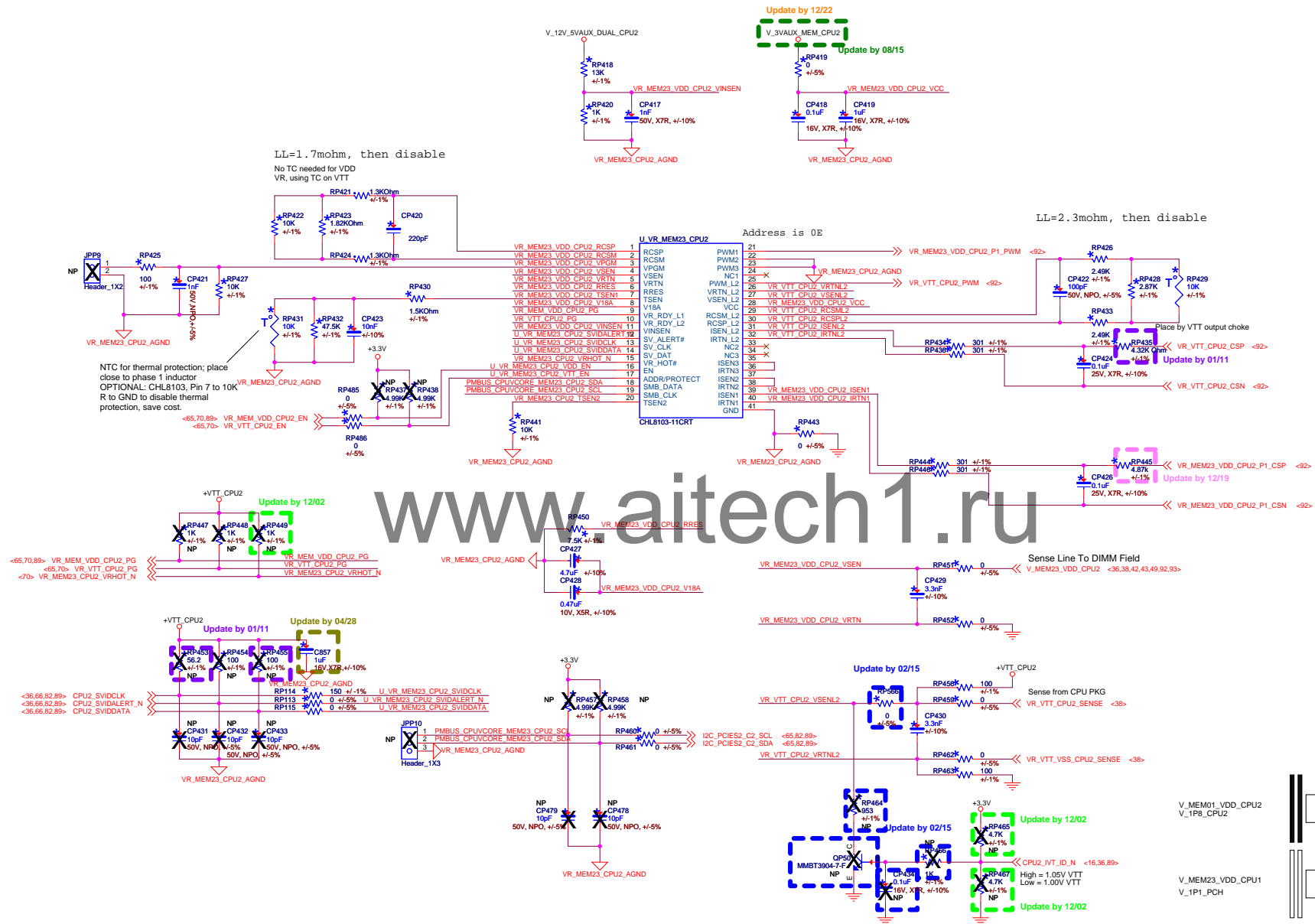
# CPU2 MEM01

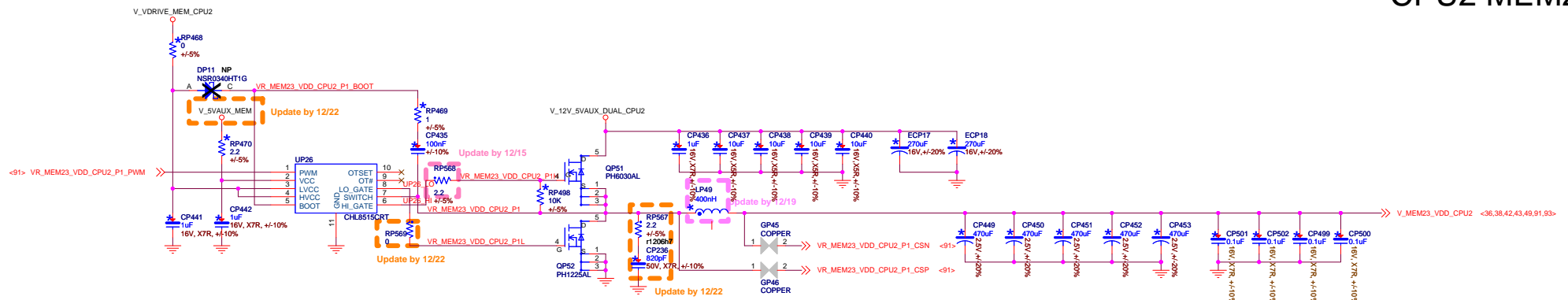


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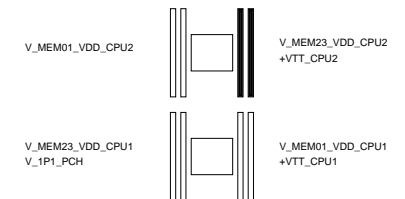
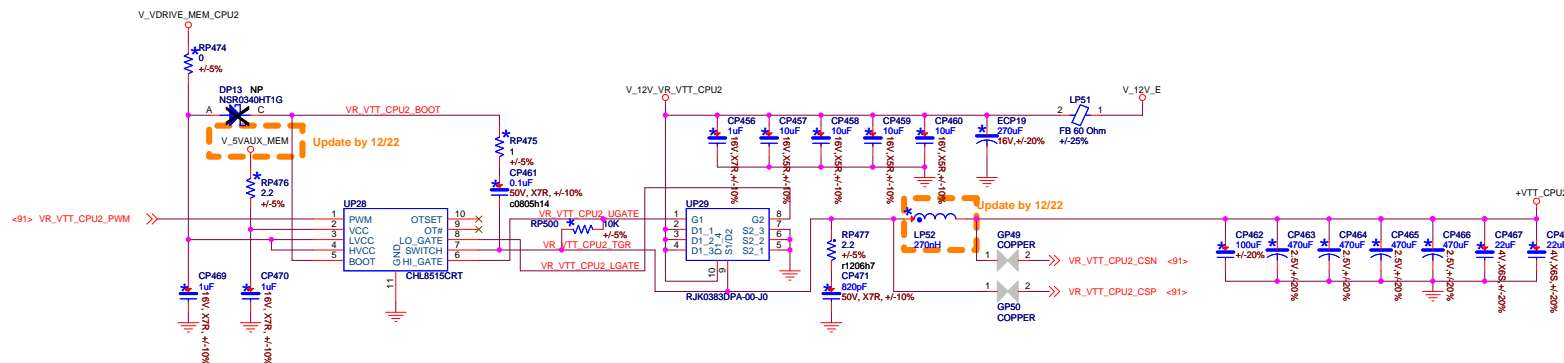


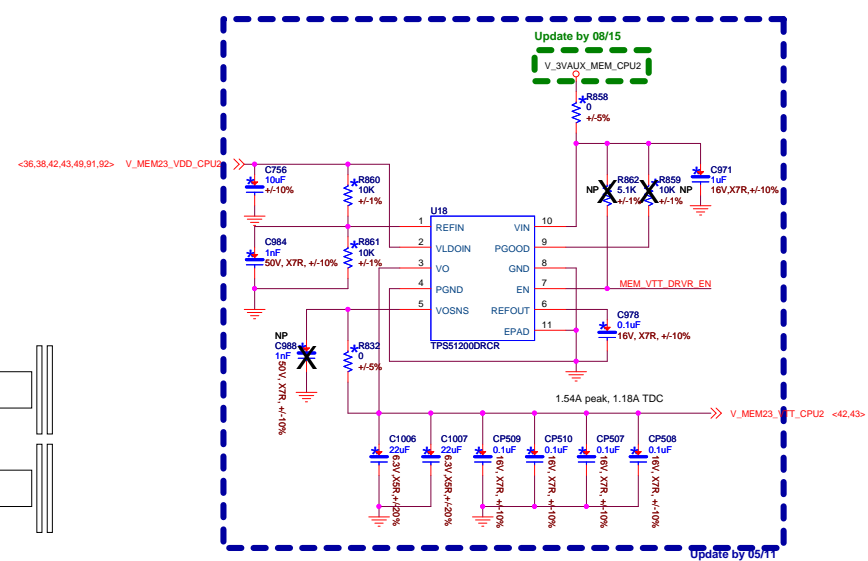
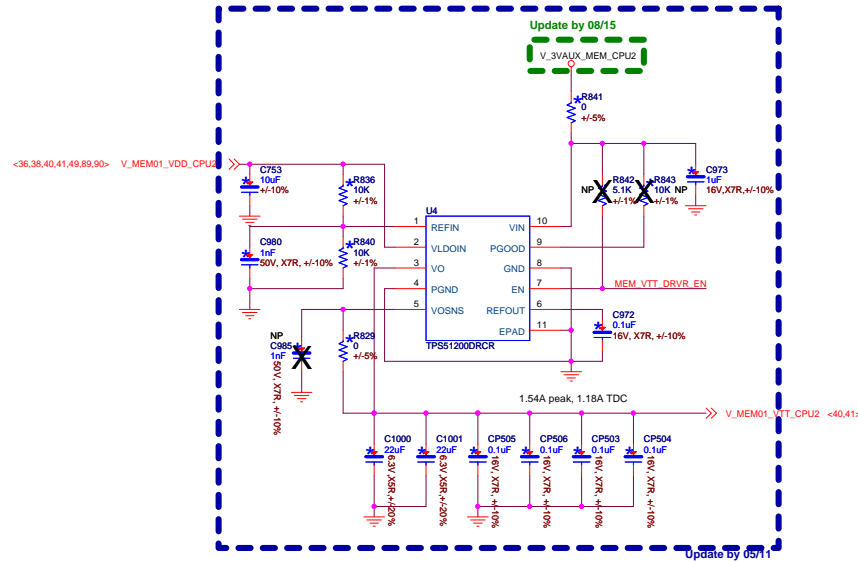
## CPU2 MEM23- CHIL CHL8103



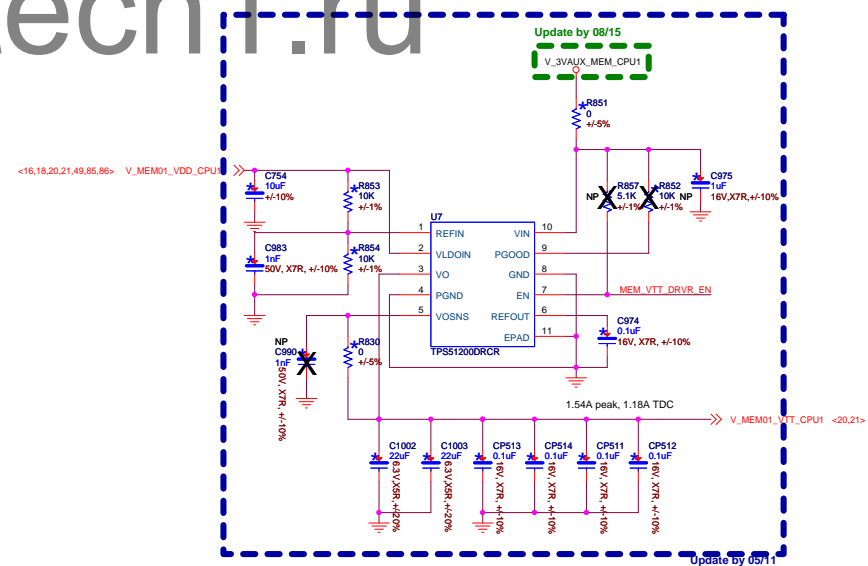
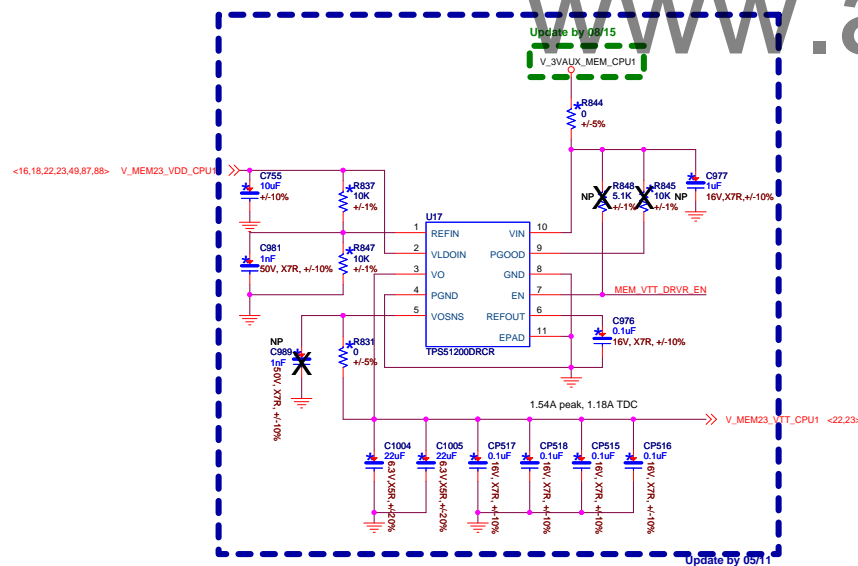


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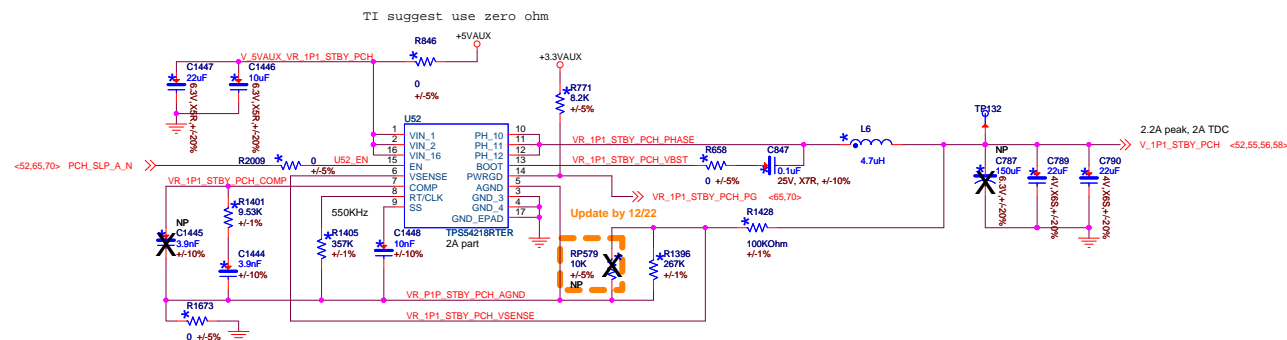


Note: VCC can be driven from V\_5VAUX\_MEM if it routes better. -jrs



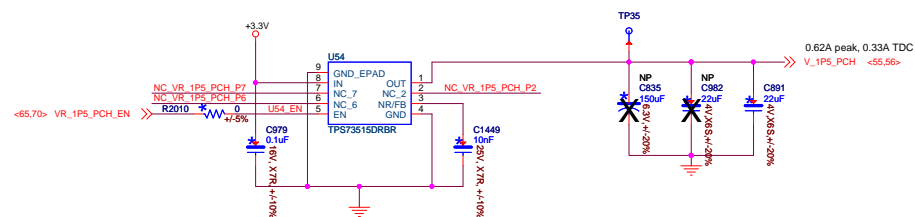


Output	V_1P1_STBY_PCH
Destination	PCH
Input	+5VAUX
Output	1.1V
Vic Current	2.4A
Max Current	2.4A
Min Load	
Min OCP	2.9A



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Output	V_1P5_PCH
Destination	PCH
Input	3.3v
Peak Current	620mA
TDP Current	330mA
OCP	800mA
Enabled	



Output	V_3P3AIUX
Destination	+5VAUX
Input	+5VAUX
Peak Current	TBD
Thermal Current	TBD
Enabled	TBD

